		milestone
V0: all interfaces fixed	2 weeks	10/06/23
V0: ASIC / FPGA / cooling design	6 weeks	11/17/23
V0: procurement (via BNL)	6 weeks	12/29/23
V0: shipments to France / Hungary	2 weeks	01/12/24
V0: whatever tests needed to initiate V1	4 weeks	02/09/24
V1: design	4 weeks	03/08/24
V1: procurement (via BNL)	6 weeks	04/19/24
V1: shipments to France / Hungary	2 weeks	05/03/24
V1: final debugging at BNL	6 weeks	05/31/24