This document describes mechanical and electrical interfaces between the components of a V0 iteration of an HGCROC3-based HRPPD readout backplane. The backplane will consist of a 1024-channel ASIC board (HRPPD_ASIC_BOARD.V0), a pair of identical FPGA boards (HRPPD_FPGA_BOARD.V0), each serving one half (512 channels) of the ASIC board, and a complementary passive interface between the ASIC board and a KCU105 toolkit (HRPPD_FMC_BOARD.V0).

1. HRPPD photosensors by Incom Inc.

High Rate Picosecond PhotoDetector (HRPPD) by Incom Inc. is a Micro-Channel Plate (MCP) vacuum photosensor of a ~119.6mm x 119.6mm x 14.1mm size (Figure **1**, left), with a fused silica window covered by a bialkali photocathode from the inside, ceramic side walls and a ceramic anode base plate, pixelated into 4x4 groups of 8x8 square pads with a pitch of 2.0mm on its outer side (see Figure **1**, center), for a total of 1024 channels. Two 600μm thick MCPs

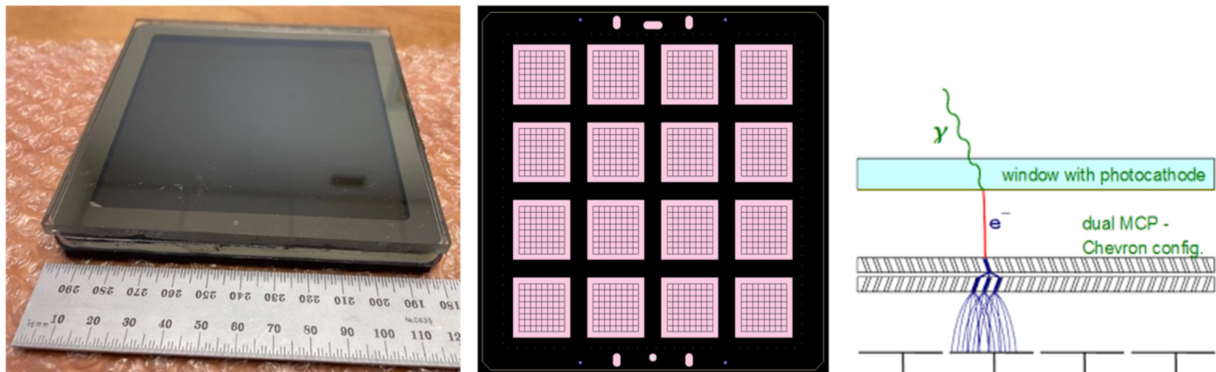


Figure 1 Left: HRPPD photosensor. Center: rear sensor side with sixteen 8x8 pad fields (gerber view). Right: Illustration of HRPPD operation principle.

provide a primary photoelectron amplification via a secondary electron emission off the narrow 10μm diameter channel walls during the "avalanche" development caused by a bias voltage up to ~1kV applied to the top and bottom surfaces of each MCP, see Figure **1** (right) for an illustration.

1.1 Mechanical interface to the ASIC board

From the mechanical point of view, the pixelated flat rear side of the sensor has six high voltage (HV) pins (https://www.mcmaster.com/95648A280/, STEP model) and 25 socket cap titanium screws (https://www.mcmaster.com/95435A207/, STEP model) with a head diameter of ~3.56mm (0.14"), either glued or brazed in such a way that the heads can be used for the ASIC board alignment with respect to the 2mm pads, and the threaded parts later on used to bolt the ASIC board onto the sensor, see Figure **2**.

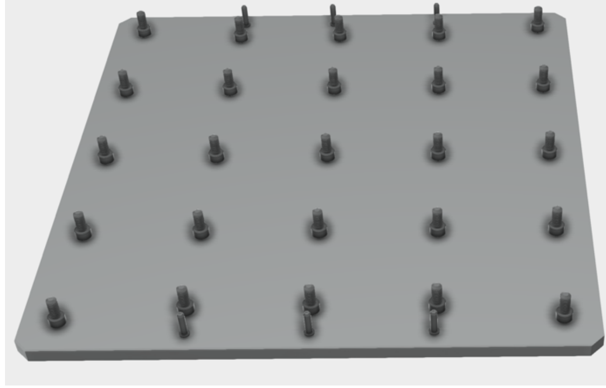


Figure 2 HRPPD anode base plate with 25 brazed socket cap screws to mount the ASIC PCB and two groups of three HV pins.

A STEP file with the model of the anode base plate with the pre-mounted HV pins and the cap socket screws is provided here. Be aware that this model is merely a mockup, while the actual *proprietary* (do not share!) Kyocera DXF manufacturing file and a pdf printout describing the High Temperature Co-fired Ceramic (HTCC) stackup of the anode base plate should be used as a primary reference for any dimensions, etc.

A 1.0mm thick 3D printed spacer between the HRPPD ceramic rear side and the ASIC PCB is described in section 1.3.

1.2 Single photoelectron pulse shape

The HRPPD is a so-called DC-coupled device, where charge is directly collected by small square pads with a pitch of 3.25mm on the inner (vacuum) side of the anode base plate. Anode in our setup is the ground level, while the photocathode is typically operated at a negative voltage up to ~2.5kV. Contrary to devices like AC-LGADs, the HRPPD gain *can be varied* during operation by changing the MCP bias voltage, and can comfortably reach few times 10^6, although a preferred setting in the experiment is perhaps few times 10^5. Single photon pulse height can reach dozens of mV (on a 50 Ohm load; depending on the gain). Pulses have leading edge <500ps (as measured from ~20% to ~80% peak value) and duration of 2-3ns, see Figure **3**.

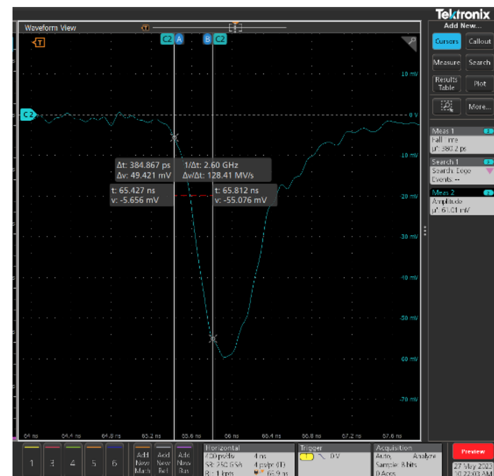


Figure 3 A typical HRPPD pulse with a leading edge ~400ps. Screenshot taken with an 8GHz ABW scope.

1.3 Electrical interface to the ASIC board

The 104mm x 104mm active area is organized as a uniform 32 x 32 3.00mm square pad field on the inner (vacuum) side of the anode plate (pitch 3.25mm). This ceramic plate not only encloses the vacuum volume but plays the role of a pre-routing PCB with a simple stack up (see Figure **4**, left), which provides an electrical connection from the uniform inner pad field to the sixteen groups of 8x8 pads with a smaller pitch on the outer side (see Figure **1**, center), in order to simplify interfacing to the ASIC PCB and provide space for the mechanical integration.

Each 8x8 pad field is surrounded by a ~2mm wide ground “band”, electrically connected to the internal ground of the ceramic stack-up (as well as to the HV ground pad), see Figure **1** (center).

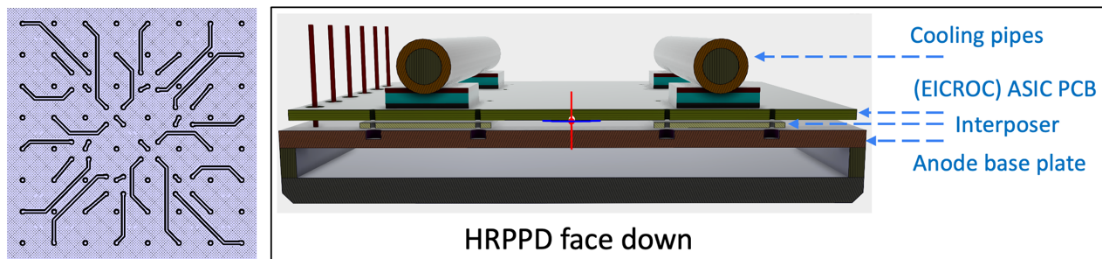


Figure 4 Left: ceramic stackup routing snapshot between 8x8 3.25mm pitch inner pads and 2.00mm pitch outer side pads (only half of the traces shown). Right: Samtec compression interposer squeezed between the sensor anode plate and the ASIC PCB (*ignore everything above the ASIC PCB in this picture).*

The electrical connection between the HRPPD sensor pads (and the internal ground) and the ASIC board is provided via custom 21mm x 21mm x 1mm size double-sided Samtec ZA1 compression interposers (model ZSP-232827-01-ZA1-D, see also Figure **5**), sandwiched between the sensor and the ASIC board during the assembly procedure, as shown in Figure **4** (right). The interposers are aligned with respect to the HRPPD base plate using 1.0mm thick 3D printed spacers with 25 3.80mm diameter holes matching the screw pattern on the sensor base plate, and a pattern of 4x4 large 21.25mm square openings matching the interposer size.

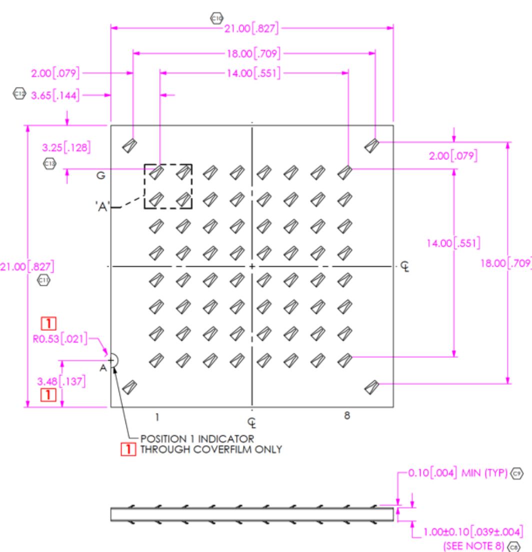


Figure 5 A custom Samtec compression interposer used with the EIC HRPPDs. Four spring pads in the corners provide a ground connection.

Traces of the internal stackup can be as long as ~10mm (see Figure **4** left, the area here is 26mm x 26mm), implemented in a 50 Ohm coplanar waveguide configuration, and have an estimated capacitance of up to ~2pF/cm (yet to be measured once Kyocera delivers the plates). Pad capacitance to ground is expected to be small. This iteration of the base plate is (somewhat unexpectedly) performed using a so-called High Temperature Co-fired Ceramic (HTCC) technology, therefore the traces are made out of a tungsten alloy rather than copper expected in a Low Temperature (LTCC) case. Since the trace cross-section is small (around 90μm x 10μm), the traces themselves will have a resistivity of up to ~1 Ohm/cm. Molybdenum alloy vias will probably add ~0.15 Ohm to this estimate. Therefore, one can expect that the resistivity of the charge flow path between the charge collecting pads and the Samtec interposer springs will vary from pad to pad between ~0.2 Ohm and ~1.5 Ohm (will be measured directly end of November 2023 once the plates are delivered to Incom). The full trace capacitance will also vary from pad to pad but should not exceed 2-3pF overall. We have no idea about the Samtec interposer contribution (will be measured directly once we have all components to assemble the whole stack).

Design drawing of the Samtec compression interposer is uploaded here, as well as a STEP model. A STEP model of a 3D printed spacer between the sensor anode plate and the ASIC board is available as well. Need to add recesses for ASIC board studs.

2. ASIC board HRPPD_ASIC_BOARD.V0

A 1.6mm thick ASIC board has a size of 119mm x 119mm with tapered corners, see the floor plan in Figure **6**. The board hosts sixteen HGCROC3 chips. Each of the ASICs serves a single 8x8 pixels spot, for a total of 64 channels. A current CAD model is uploaded here.

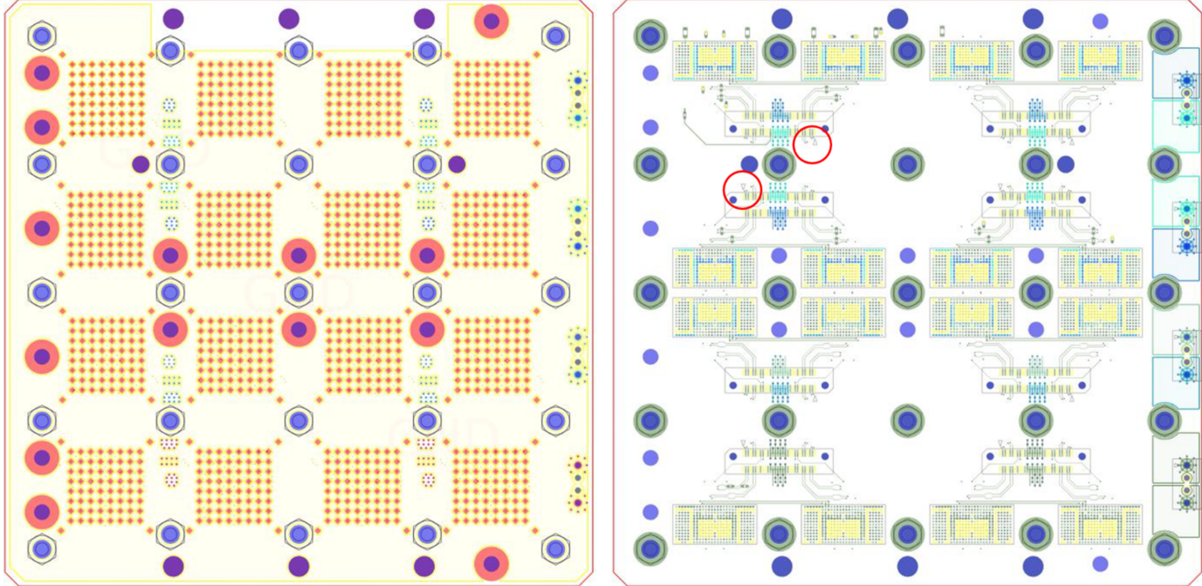


Figure 6 HRPPD_ASIC_BOARD_V0 layout. Left: bottom (HRPPD) side. Right: top (ASIC) side. Pin 1 locations are encircled in red.

2.1 Mechanical and electrical interface to the HRPPD sensor

The ASIC board is bolted onto the HRPPD rear side (anode plate) by 25 socket cap screws, see section 1.1. As seen in Figure **6** (left), the board should therefore have respective 4.00mm diameter through holes (shown in blue) matching the location of the screws on the sensor rear side, and also six 4.00mm diameter holes (shown in purple) in order to not interfere with the sensor high voltage pins. See the CAD model and Figure **7** for the exact locations. A stay clear area around the screw caps on the top side of the ASIC board should be 7.0mm, at a minimum. As described in section 1.3, the HRPPD pads are routed to the bottom side of the ASIC readout board via double sided Samtec compression interposers. The ASIC board should therefore have a matching pattern of 1024 spots on its bottom side, as well as the four ground spots per each of the 4x4 64-pad groups, see Figure **6** (left). A bare board CAD model is uploaded here.

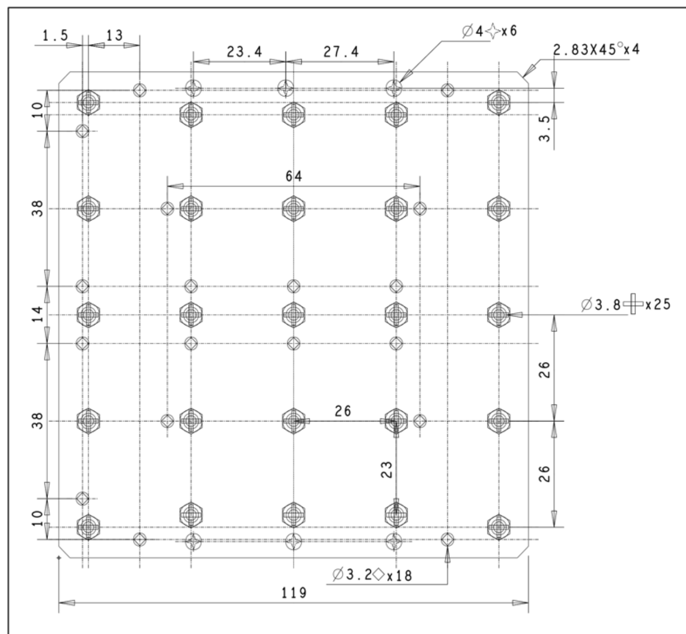


Figure 7 ASIC board mechanical hole pattern.

2.2 Mechanical and electrical interface to the FPGA (FMC) boards

Control of the ASIC boards will be done via a pair of independent and identical mezzanine FPGA (or a dummy FMC) boards described in sections 4 and 5. Each of the two FPGA (FMC) boards will serve eight HGCROC3 chips as shown in Figure **8**.

We will use matching 2x30pin Samtec ERM5 (male: ERM5-030-05.0-L-DV-TR, STEP file) and ERF5 (female: ERF5-030-05.0-L-DV-K-TR, STEP file) board-to-board connectors between the ASIC board and the FPGA board. The ERM5 (male) ones will be used on the ASIC board. See the CAD model for exact locations. Every two HGCROC3 ASICs will share one ERM5 connector (see Figure **6**, right). *No trigger lines will be used between ASICs and FPGA boards*.

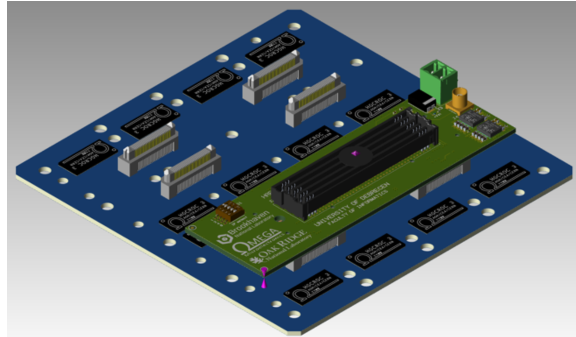


Figure 8 One of the two FMC boards mounted on top of the ASIC board.

Pin 1 locations are indicated in Figure **6**. Pin designation is shown in Figure **10**. We will use 1 CLK and 1 FCMD line per ASIC. The I2C bus will be common for every two chips. ASIC chips served by the same FPGA will have identifiers in a range from 0 to 7 as shown here.

FPGA & FMC boards will be snapped onto the ASIC board and mechanically aligned with respect to it by means of the ERM(F)5 connectors. Besides this, each of the FPGA boards will be (optionally) fixed in situ by a pair of PEM KFH broaching studs (see p.12), which will be pre-mounted onto the ASIC board in a way shown in Figure **9** (center) (will use 3.2mm diameter isolated plated through holes). We assume a 18mm long KFH-M3-18ET stud model will be used, with standard hexagonal M3 nuts (Ø6mm clearance on the top side of FPGA board required, see Figure **9** right). Holes in the FPGA board should match the M3 thread diameter.

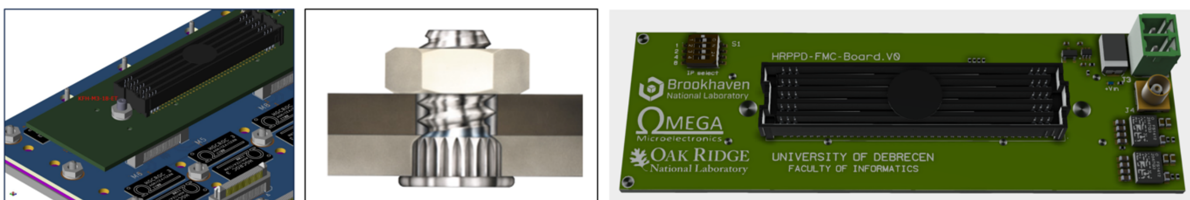


Figure 9 Left: FMC board fixed in situ by KFH studs. One can also see three HV pins on top of the picture and a pair of HRPPD screws on the left. Center: PEM KFH broaching stud (here shown in a configuration without a gap between the two boards). Right: A 3D model of the FMC board. Location of the mechanical holes for broaching studs is indicated by circles on both sides of the HPC connector.

Low voltage power distribution to the ASIC boards will be provided in two different ways:

- FPGA boards will have an LV connector (see Figure **9**, right) and a set of LDOs, and will feed both analog and digital power to the ASIC board via a set of designated pins in each Samtec ERF5 connector (see Figure **10**);
- The same functionality is foreseen for the “passive” FMC boards, see section 4;
- Besides this, ASIC boards will have their own LV connectors (one per a row of ASICs), and *power will be taken from this connector if the respective cable is plugged in*
- ASIC (?), FMC and FPGA boards will all use the same LV connector

2.3 Mechanical interface to the cooling cold plate

It is expected that each ASIC will dissipate at most 15mW of power per channel. Active air cooling will be provided by aluminum cold plates with fins directly attached to the ASICs via soft gap pads (?; reference), see section 0. The details of the cooling setup are not fixed yet, but it is agreed upon that (as indicated in Figure **6**), the ASIC board should have eight 3.2mm diameter isolated plated though holes (shown in pink) to attach cooling system cold plates via the same type of KFH broaching studs used to bolt the FPGA boards to the ASIC board, as explained in section 2.2. See a Figure **7** for the exact location of these holes. ASIC board will have a ~5mm x 5mm bare copper spot in a top left corner (see Figure **6**) to solder a braid for grounding the cold plate.

1	GND	2	GND
3	DAQ1_M2_n	4	CLK320_M2_p
5	DAQ1_M2_p	6	CLK320_M2_n
7	GND	8	GND
9	DAQ0_M2_p	10	FCMD_M2_p
11	DAQ0_M2_n	12	FCMD_M2_n
13	GND	14	GND
15	S_RSTb_M2	16	NC
17	H_RSTb_M2	18	GND
19	GND	20	GND
21	NC	22	NC
23	AVDD	24	DVDD
25	AVDD	26	DVDD
27	AVDD	28	DVDD
29	AVDD	30	DVDD
31	AVDD	32	DVDD
33	AVDD	34	DVDD
35	AVDD	36	DVDD
37	TRIG_G1	38	NC
39	GND	40	GND
41	GND	42	GND
43	H_RSTb_M1	44	SDA_G1
45	S_RSTb_M1	46	SCL_G1
47	GND	48	GND
49	DAQ1_M1_n	50	CLK320_M1_p
51	DAQ1_M1_p	52	CLK320_M1_n
53	GND	54	GND
55	DAQ0_M1_n	56	FCMD_M1_p
57	DAQ0_M1_p	58	FCMD_M1_n
59	GND	60	GND

Figure 10 Description of the 2x30 pins of the Samtec ERF(M)5 connector.

2.4 Trigger signal digitization

For the purposes of timing synchronization across all FPGA boards in the system, each group of two ASICs connected by the same Samtec connector to the FPGA (FMC) boards will use a single channel in a range from 64 to 71 in one of the ASICs to digitize a reference timing pulse. This pulse will be derived from a TTL trigger signal fed into an MCX connector on the FPGA(FMC) board (see section 3), shaped by the FPGA, and propagated to the ASIC board via a designated TRIG_Gx pin in each of the Samtec ERF5 connectors. The leading edge of this signal (a level drop from +1.2V to 0V) defines the timing reference. The width of this signal should be >500ns and be configurable via FPGA I2C interface together with the delay. These signals will be fed into the respective ASIC input via a serial 2pF capacitor. In case of the FMC board, the scheme is the same: the TTL signal is fed into the KCU105 card FPGA via a Twinax cable, and back to the ASICs.

3. FPGA interface

Interface between the ASIC board and a host DAQ system will be provided in two different configurations: via a dummy (FMC) interface board described in section 0, and a more advanced FPGA board described in section 5. A dummy interface board will only provide a connection to a KCU105 kit, while the FPGA board will also allow for a direct connectivity to a host DAQ PC via both USB3 and gigabit ethernet links.

Either the FMC or FPGA boards will serve eight ASIC chips and will be completely independent from each other. They should have a +5V LV connector and provide a default LV power to the ASIC board via Samtec ERF5 connectors, see also section 2.2.

Both implementations will have a fully functional external trigger interface. A host DAQ will feed a TTL trigger signal with a minimal duration of 100ns into a single female MCX connector on either the FMC or FPGA boards. Leading edge of this signal defines the L1A FCMD timing. A derived analog signal to the ASIC board for the purposes of timing synchronization will be also created, see section 2.4. Since this derived signal will be delayed with respect to the prompt pad signals (“real” HRPPD hits), the FPGA will issue a sequence of two fast commands per trigger, with an independently configurable delay.

We are going to use a Kintex Ultrascale (XCKU040) on the FPGA board, also in order to be fully compatible firmware-wise with the KCU105 development kit. A KCU105 will provide both USB3 and ethernet interface otherwise missing on the FMC board. Therefore, the FPGA firmware as well as the interface to a host DAQ PC will be very similar if not identical in both ASIC+FMC+KCU105 and ASIC+FPGA board configurations.

The only data acquisition mode of interest is a single event triggered mode (no buffering), where a host DAQ guarantees a proper VETO functionality in its fast logic scheme (no spurious trigger signals before the current event is fully read out).

Either ASIC+FMC+KCU105 or ASIC+FPGA configurations should provide both USB3.1 and 1Gb ethernet connectivity (~950Mb/s with Jumbo frames, Ethernet PHY:KSZ9131RNX) to the host PC, with the following minimal functionality:

- HGCROC3 ASIC configuration via I2C
- Configuration of the timing synchronization pulse (derived from the external trigger)
- Generation of a configurable L1A FCMD pair via a software command
- Generation of a configurable L1A FCMD pair upon receipt of a hardware trigger signal
- A single event data transfer to the host PC

Format of the event record is yet to be defined.

All connections (LV, USB, Ethernet, MCX) on the FPGA (FMC) boards will be vertical, to simplify HRPPD tiling with a minimal interference between the neighboring sensors.

4. Dummy interface board HRPPD_FMC_BOARD.V0

As a backup and a test plan option, we will build a “simple board” which replaces the FPGA board and provides a standard VITA57/FMC connection (ASP_134603_01), which allows us to use a KCU105 development kit for first tests of the ASIC board. This board has a 105mm x 33mm size, is 1.6mm thick, and will be mechanically compatible with the FPGA board HRPPD_FPGA_BOARD.V0 in terms of:

- location of the Samtec ERF5 connectors
- location of the two mounting through holes for the KFH studs

Figure 11 Samtec cable to provide connectivity between a HRPPD_FMC_BOARD.V0 board and a KCU105 kit.

We are going to use a standard Samtec FMC cable (HDR-169470-01) to provide connectivity to a KCU105 development kit, see Figure **1512**.

It is expected that this board will be typically used in a configuration with only a few powered up ASIC chips. Therefore, no cold plate and no cooling fan will be used, and as such no mechanical compatibility between the Twinax cable and the cooling system is required. This board should provide LV to the ASIC board, in the same way the FPGA board does. It will distribute the trigger signal via an onboard female MCX connector the same way the FPGA board does. Pin-out of the FMC connector, of the four Samtec connectors, as well as the schematics of the trigger input is provided here and here. Stackup, component placement and critical dimensions are available as well. STEP file is provided here, as well as a full fabrication package. See also Figure **1613**, and images of the top and bottom sides in Figure **1714**. See also a 3D model in Figure **9** (right).

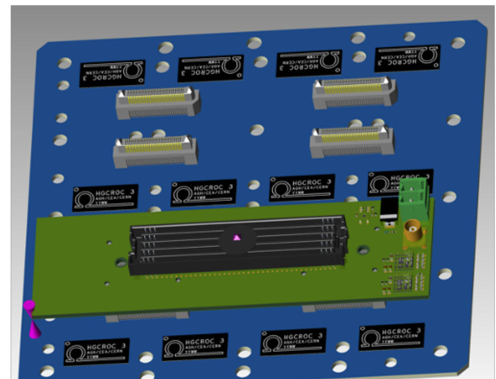


Figure 12 HRPPD_ASIC_BOARD_V0 with one HRPPD_FMC_BOARD.V0 mounted.

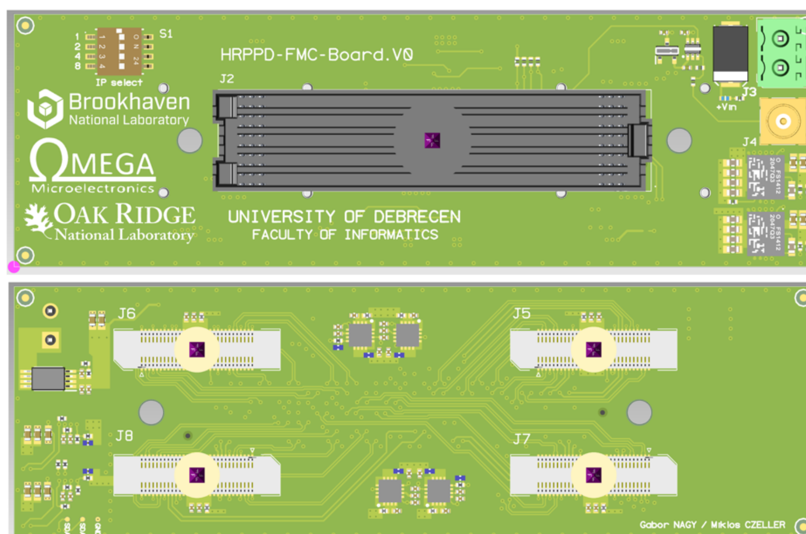


Figure 13 HRPPD_FMC_BOARD.V0 board (top and bottom sides).

5. FPGA interface board HRPPD_FPGA_BOARD.V0

This section is under construction

It is anticipated that the FPGA control board can fit into 1??mm x 33mm, see Figure **1411**, and have thickness of 1.6mm.

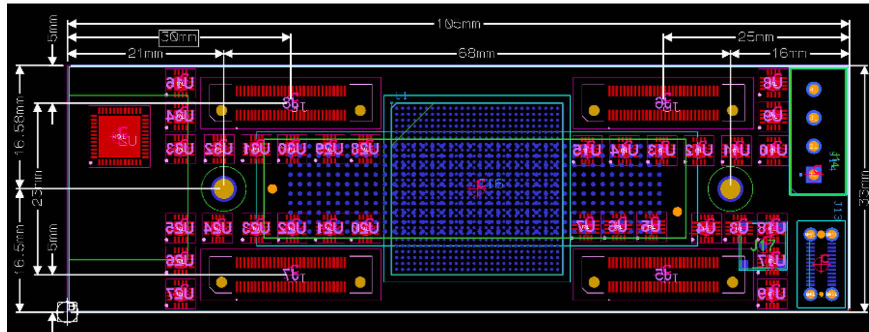


Figure 18 Layout of the HRPPD_FPGA_BOARD.V0. Need a new picture.

This board provides an interface between eight HGCROC3 chips of the ASIC board and the data acquisition PC. For the overall board layout see Figure **8**. For the mechanical and electrical interface to the ASIC board see section 2.2.

3.1mm diameter unplated through holes for the cold plate mounting studs.

A dipswitch to select four lower bits of the IP address.

6. Cooling system setup

Air cooling will be realized by installing a set of three separate aluminum cold plates with fins, which will be directly attached to the ASICs, FPGAs and other power dissipating components (?), presumably via appropriate soft pads (?). Mechanical connection to either the ASIC board or FPGA boards will be made by KFH broaching studs (eight for the ASIC board heat sink and two for each of the FPGA boards), see also section 2.2. A single 92mm diameter fan will be used for each HRPPD sensor assembly consisting of a sensor itself, an ASIC board and a pair of FPGA boards.

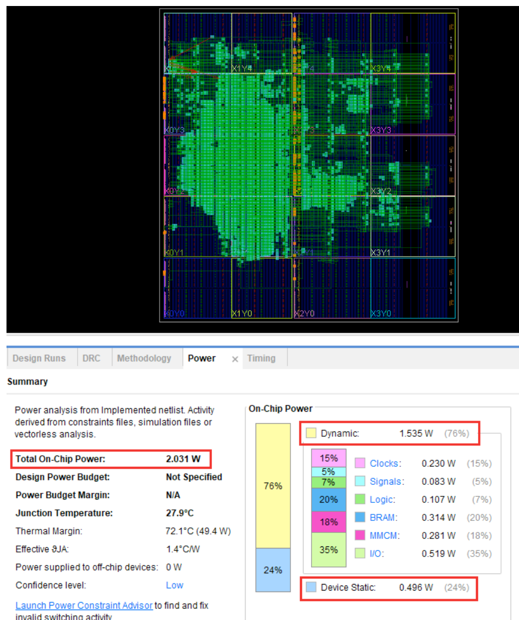


Figure 19 FPGA power estimate.

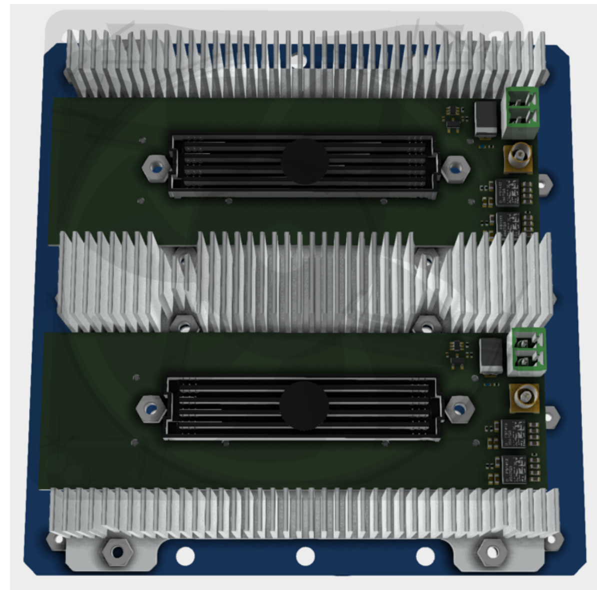


Figure 20 A tentative cooling system setup, shown with a fan masked out (FMC board configuration).

A full power budget of such an assembly is expected to be close to 30W, with <1.2W per ASIC, <2.3W per each of the two FPGAs (see Figure **1915**, where ethernet connection support will increase the current estimate by ~10%), ~1W per each of the two on-board Ethernet interfaces, and a ~90% efficiency of the DC-DC convertors.

A preliminary CAD model is shown in Figure **2016**. See also a heat sink CAD model separately.

6V power (?) to the fan will be provided via an on-board header on the FPGA board.

N temperature sensors (model) will be installed per HRPPD assembly in the ASIC+FPGA board configuration. Temperature control will be performed by FPGA firmware, with an LV power shutdown functionality upon reaching a configurable temperature threshold to be implemented in the FPGA board circuitry.

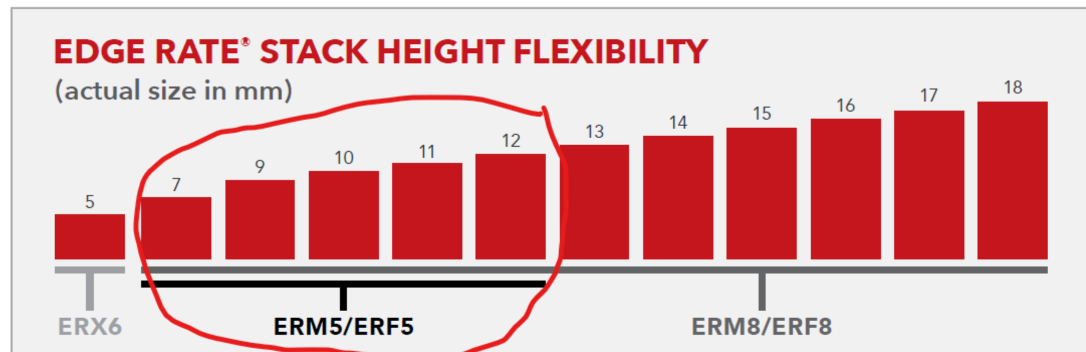
The details of this system will be defined once the mechanical layout of the ASIC and FPGA boards is decided, and in particular the height of the ERF(M)5 connectors is agreed upon, as defined by the size of the active components (2..4mm height expected).

7. Appendix

	Parameter	Comments
FPGA-ASIC board interface		
Differential signal standard	DIFF_SSTL12_DCI	
LVDS<->CLPS level convertors	none	
Termination of the CLK and FCMD lines	Done on the ASIC board	
Termination of the DATA lines	Done inside of the FPGA	No additional resistors required
DAQ signal interface	MCX female	
Trigger signal (FPGA boards)	TTL, 100ns minimum, leading edge from ~0V to +2.5V	
Timing reference (ASIC board)	500ns minimum, leading edge from +1.2V to 0V	Derived from the trigger TTL signal

8. Spares

(if needed the EFR5/ERM5 connectors has a different height option up to 12mm)



It's important to do a real BOM list with all PCB, connectors and mechanical parts needed. Actually, my board is called 2310_Hrppd_Asic_Board and Y05 for Alexander card.