SMD Commissioning Offline Analysis Suggestions

RIKEN/RBRC

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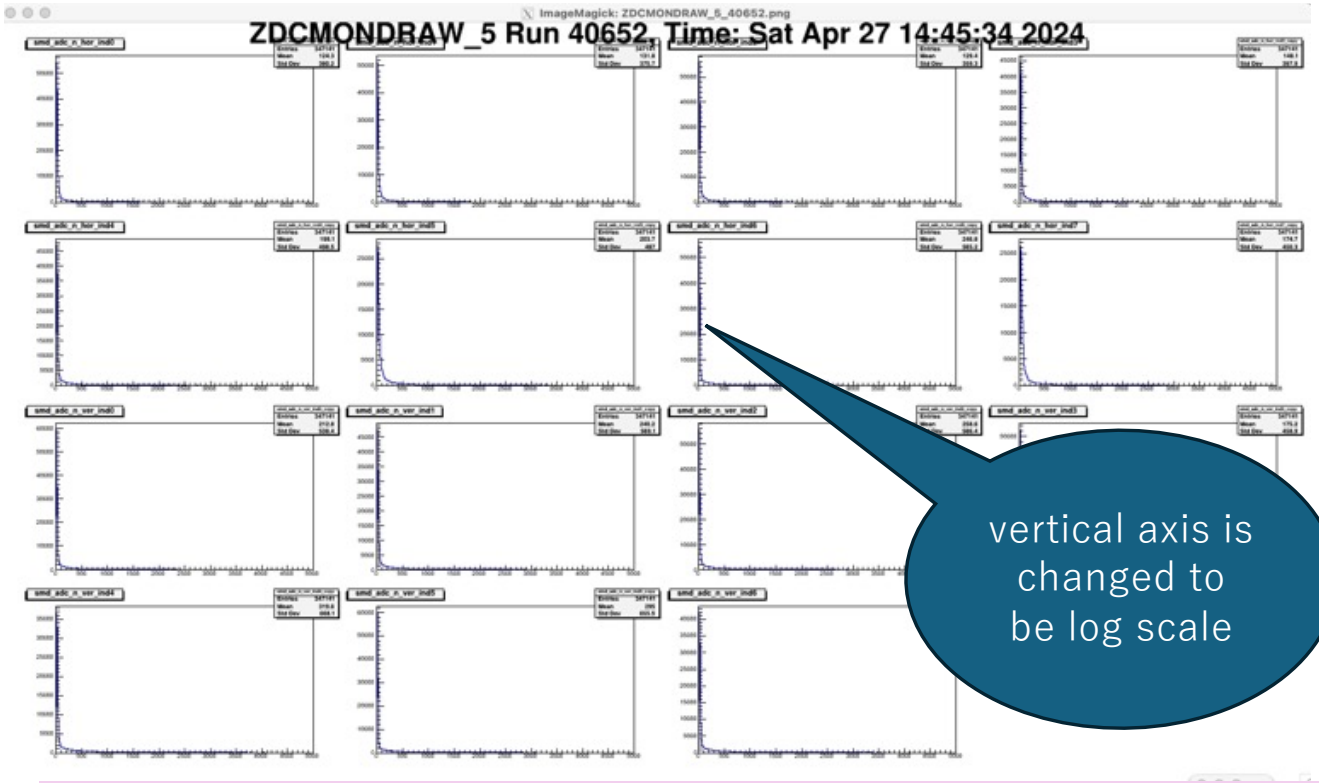
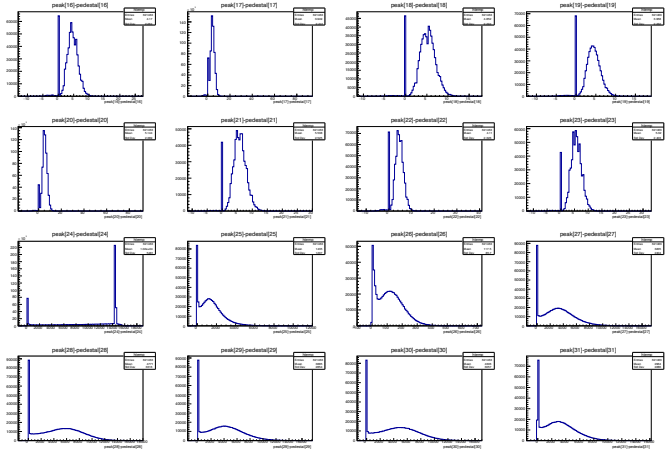
Data

- Run#40562
- April 27, 2024 14:40 ~ 15:25?
- Trigger : ~450Hz @ ZDCNS Coincidence (after ZDC HV and threshould tune).

SMD ADC spectra

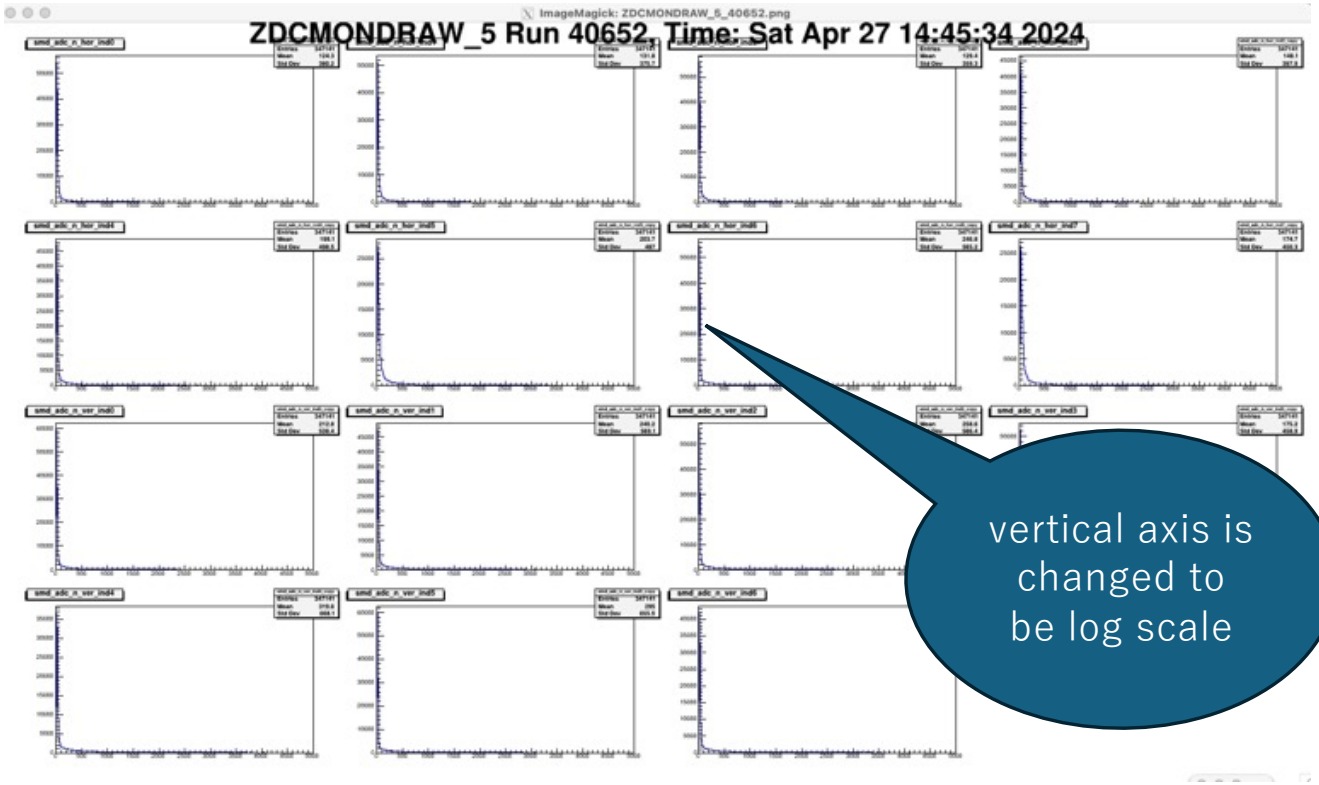


↑ North SMD ADC spectra of Run#40652 from p+p @ Run24. Pedestal dominates the entries and signal peaks are invisible with linear vertical scale. This is because number of paddles fired by single neutrons are typically 2 or 3 and rest of paddles are just observing pedestals. Need to change the vertical scale to be log.



↑ North SMD ADC spectra of Run#24787 from Au+Au @ Run23. Signal peaks are visible together with pedestal. This is because of shower caused by multiple neutrons which illuminates more paddles.

SMD ADC spectra



M.J.Kim Ph.D Thesis

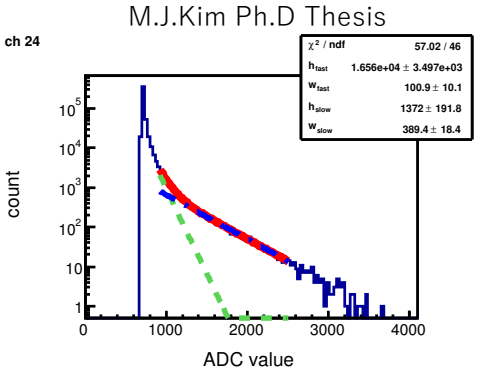
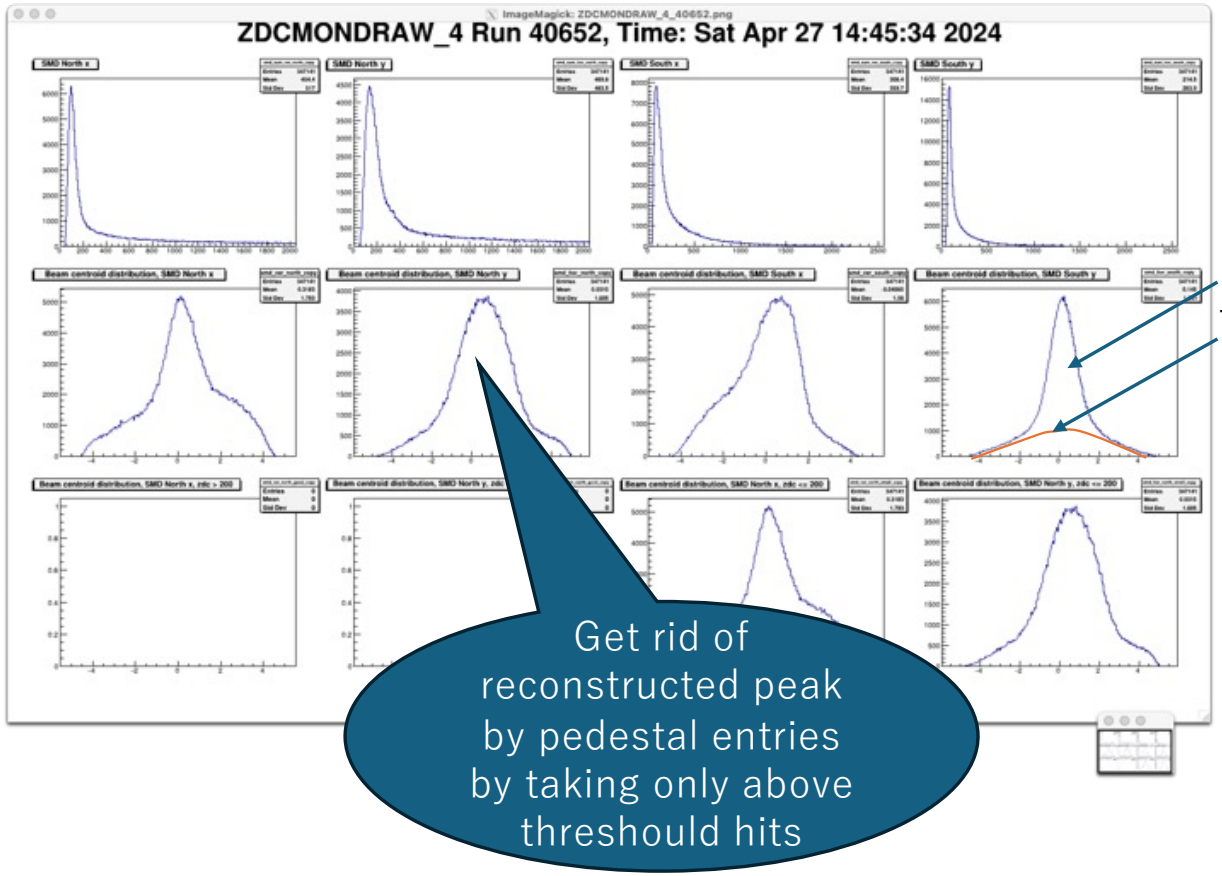


Figure 5.5: Eq. 5.2 fitting result of a strip.

↑ This is how SMD ADC spectrum looks like in p+p. Please confirm if the right plot becomes like above once vertical axis is give in log scale.

x,y position Reconstruction

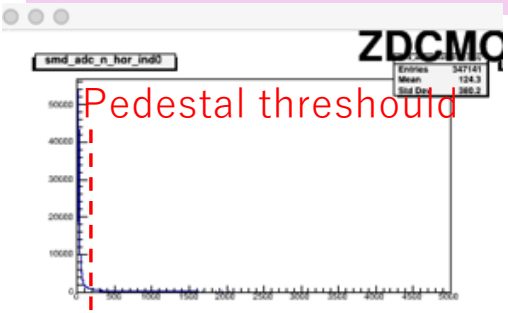


- Reconstructed x,y distribution seem to have two components.
- They look the superposition of pure pedestal narrower and true neutron peaks.
- The broader peaks may be the true neutrons since it shows symmetric in y-direction and left-right asymmetric in x-direction.

Pedestal?

True Neutron?

- We should apply pedestal cut on SMD ADCs and use only hits above the threshould for all SMD paddles and get rid of reconstructed peak by pedestals.



Energy Distribution

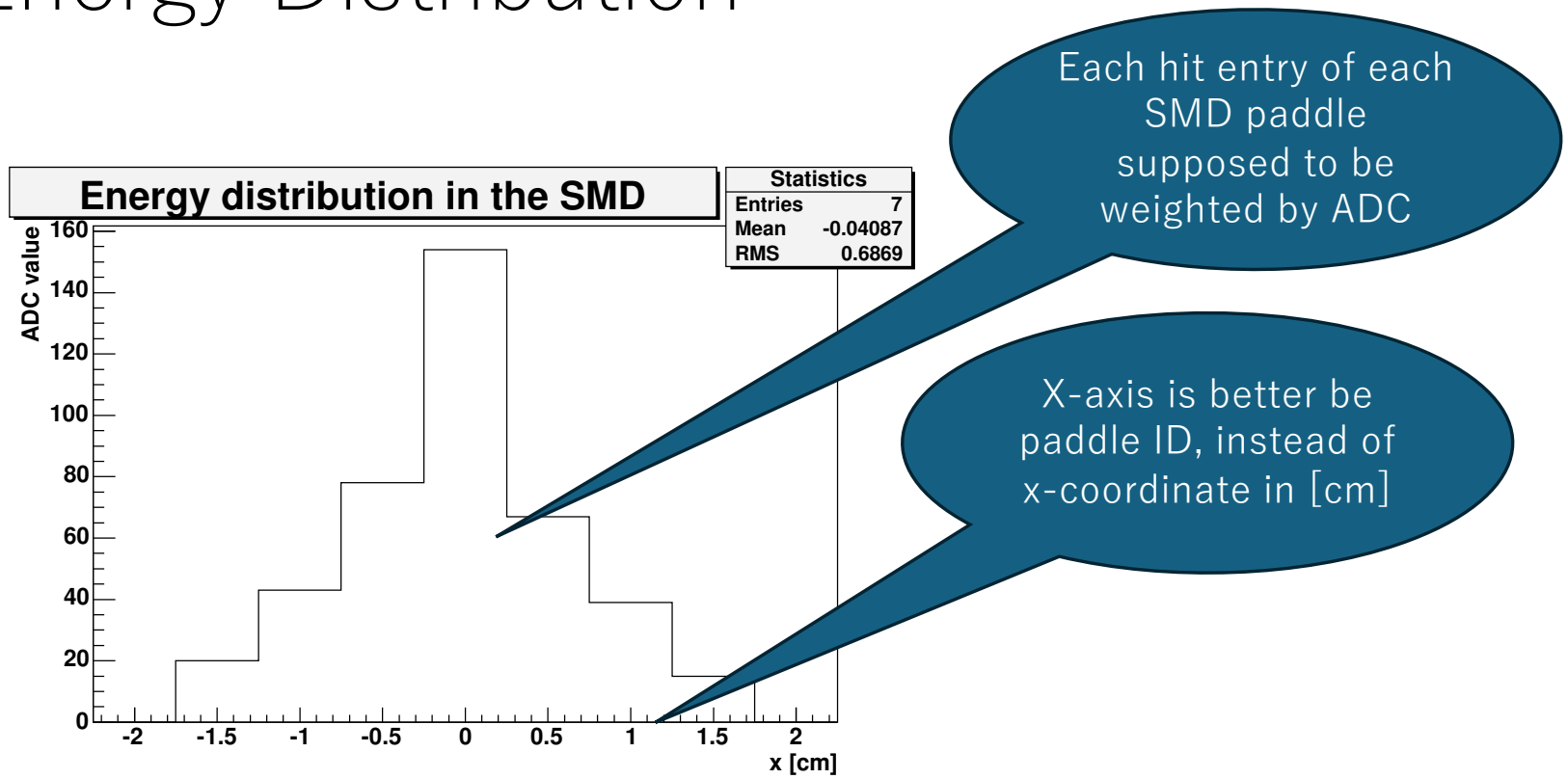
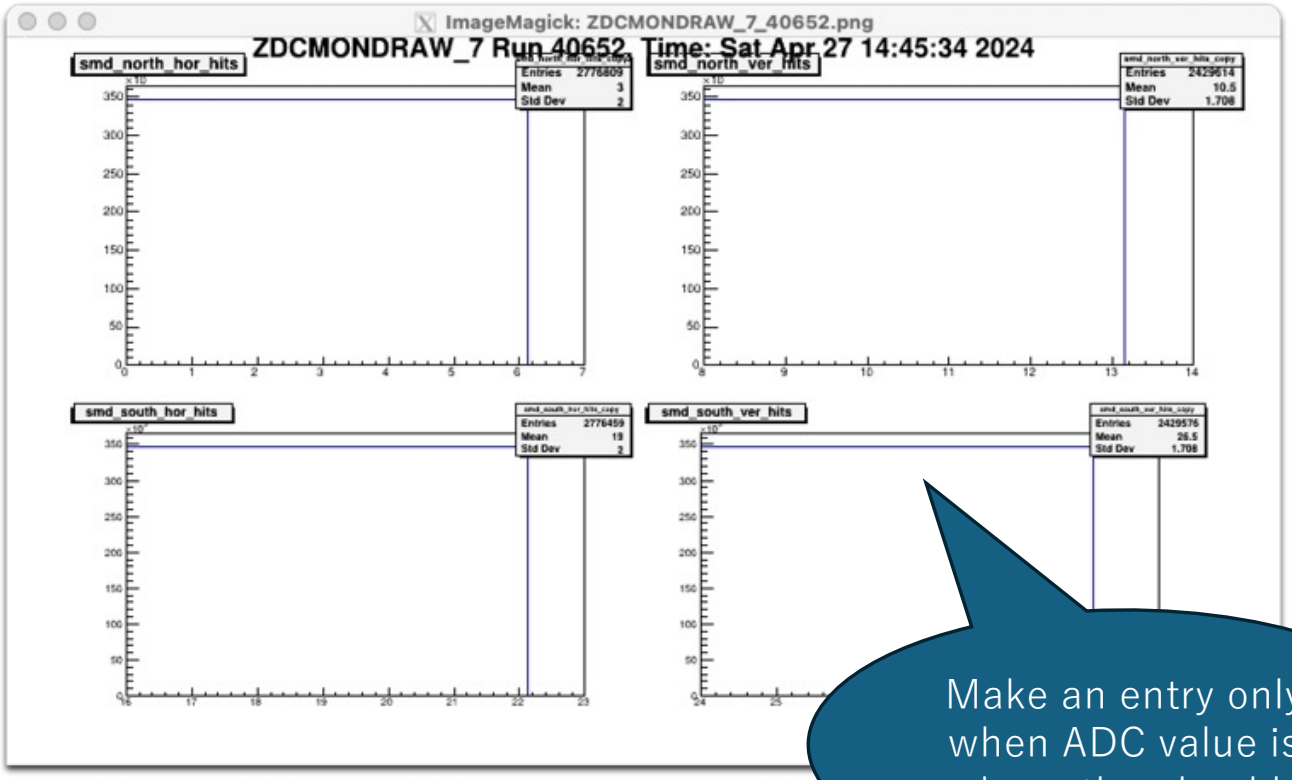


Figure 2: SMD energy distribution

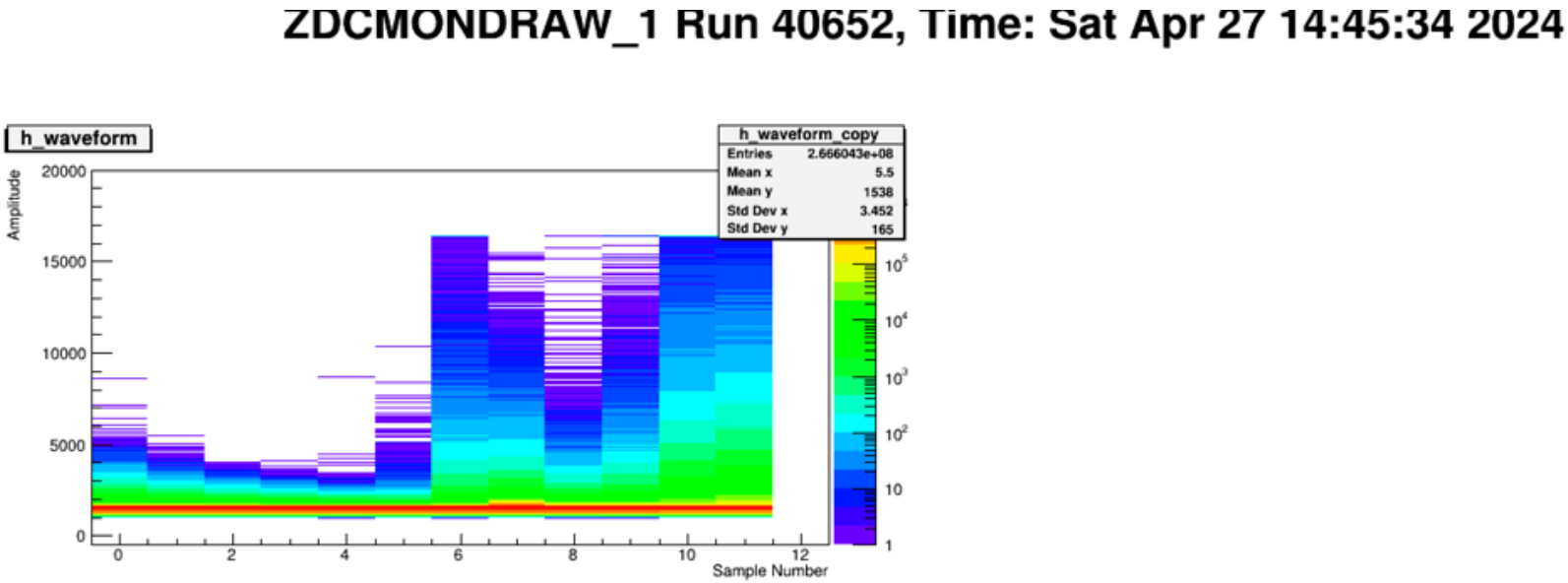
Hit Multiplicity



Make an entry only when ADC value is above threshould.

- Somehow the distribution is just flat.
- This is probably because hits are counted for every events. Each counter has at least finite pedestal, thus all paddles ends up with same entry.
- We should fill the histogram only when ADC value is above threshould.
- The distribution is expected to be peaked around center.

Wave form



I am not sure if the ADC timing is correctly tuned at this moment.