Zynq VME Controller Specification

DRAFT Version 0.9 May 1, 2018

1. Introduction

This document describes a proposal for a Xilinx Zynq based VME controller card design.
This design is intended to replace, upgrade and extend the lifetime of the VME based Front End Computing hardware now deployed in the accelerator complex. The goal is to provide a versatile platform that could replace the basic FEC installation with a single slot card and support the VME interface to cover the full range of configurations with existing custom VME cards. New installations can be supported with the new controller and off-the-shelf and custom FMC mezzanine cards. This document contains information needed to select features and estimate area and power. It will evolve into a controlled design specification.

2. Features

• Zynq-7000 XC7Z045-2FFG900C AP SoC

• Artix XC7A50T-2FGG484I

• VME32 Interface

• VITA 57.1 FMC HPC connector

• VITA 57.1 FMC LPC connector

• 1 GB DDR3 component memory (four 256 Mb x 8 devices) connected to the processing system (PS) side

• Two 256 Mb Quad-SPI (QSPI) flash memory chips connected to Zynq (64 MB) .

• One 256 Mb Quad-SPI (QSPI) flash memory chip connected to Artix (32 MB).

• IIC EEPROMs connected to Zynq and Artix (4 KB). Available to store version information, MAC address, serial numbers, etc. Zynq PS or PL can access.

• USB 2.0 ULPI (UTMI+ low pin interface) transceiver with micro-B USB connector.

• Micro Secure Digital (microSD) card connector.

• JTAG interfaces to Zynq and Artix via 14 pin headers.

• Clock sources:
  ° Fixed 33.33 MHz LVCMOS PS oscillator (single-ended)
  ° Fixed 200 MHz LVDS oscillator (differential)
  ° I2C 10 to 800 MHz programmable LVDS PL oscillator (differential)
  ° External PL clock on SMC connectors (differential)

• Ethernet PHY RGMII interface with RJ-45 connector on front panel.

• RS232 interfaces via USB A connectors to Zynq and Artix on front panel.

• Small form-factor plugable plus (SFP+) connector (front panel)

• GTX transceiver support:
  ° FMC LPC connector (one GTX transceiver)
  ° FMC HPC connector (eight GTX transceivers)
  ° SFP connector (one GTX transceiver)

• I 2C bus multiplexed to:
  ° 1-to-16 TCA6416APWR port expander
  ° M24C08 EEPROM (1 kB) (board data)
  ° RTC-8564JE real time clock
  ° FMC HPC connector
  ° FMC LPC connector
  ° Si570 clock

• Eight Status LEDs (front panel):
  ° Power Good(s)
  ° FPGA DONE(s)
  ° One Zynq user LED

• Three “Blue Hose” Link connections, eight 3.3V GPIOs and eight buffered 12b ADC inputs on unused VME pins.

• Six additional power/ground pairs on spare VME pins. Could allow maximum utilization of XC7Z045. (45W x 2)

• AP SoC PS Reset Push button on front panel.

• Configuration options:
  ° Dual Quad-SPI flash memory
  ° 14-pin PL JTAG header
  ° Secure Digital (SD) micro card

• On-board temperature sensor via XADC

• Sequenced power up/down.

3. Detailed description

The Zynq VME Controller design is based on the Xilinx ZC706 evaluation board. The format is 6U single slot. Power is supplied from the VME backplane. The Zynq FPGA on the board includes dual ARM processors and abundant programmable logic resources. An Artix FPGA was added to provide the VME interface function. The board provides power, clocks and IO to two FMC cards.

3.1 VME Interface

The design supports the VME32 specification for 32 bit address and data. That includes support for 16 and 8 bit data, 32, 24 and 16 bit addresses, interrupt controller, bus arbitration, master /slave and system controller functions. The VME interface control will be implemented in an Artix FPGA with its own boot flash and clock. Open drain pull-ups and terminations are on the backplane.

3.2 Artix XC7A50T

The Artix is wired to VME bus buffers, IIC EEPROM, RS232 and 32 MB Quad SPI flash memory. It has its own 14 pin 3.3V JTAG header. It boots from QSPI flash triggered by power up or signals from the Zynq. All IO banks are powered from 3.3V except bank 15 which is supplied from 1.8V and is where an eight bit Zynq SPI bus and a Zynq interrupt line is connected. The Zynq SPI bus is a path for the Zynq to update the Artix's configuration flash. The Zynq can drive the Artix PROG_B and INIT_B pins and monitor its DONE_B pin. The Artix shares a fixed 200 Mhz clock with the Zynq. It also shares MGT transmit clock and data lines with the Zynq to provide a high speed communication path. The Artix may support a state machine and/or a Microblaze VME controller. VME bus access could be on command from the Zynq or autonomous.
Eight 5V op-amp buffered ADC channels with programmable are wired to the 12b XADC in the Artix at bank 15. The XADC uses an external 1.25V reference.The gain is set to 1/5 to obtain maximum 1 Vp XADC range. The maximum common mode input to XADC is 0.5V which can be adjusted by divider from the 4V DAC reference. The eight channel offset DAC has a 0 to 4V range. Op-amp outputs should have a protection diode. 5V/2exp12 = 1.2 mV/bit best resolution. XADC AUX pins connected will probably be used in unipolar mode. Input impedance is selected with resistors. The buffer amplifiers are wired to spare VME pins

3.3 Zynq Features

- Zynq-7000 XC7Z045-2FFG900C AP SoC
- Dual-core ARM® CortexTM-A9 based processing system (PS) and 28 nm Kintex-7 FPGA (PL) -2 800 MHz capable, clocked at 667 MHz
- USB, Ethernet, SPI, SD/SDIO, I2C, CAN, UART, and GPIO
- 350K cells, 218,600 LUTs, 437,200 flipflops,
- 19.2 Mb block RAM, 900 DSP slices
- 2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs
- 128 PS IO, 16 GTX IO, 212 PL HR IO, 150 PL HP IO
- 128 Switch selectable boot from microSD, QSPI Flash or JTAG

3.4 RAM

The design includes 1 GB DDR3 SDRAM wired to the Zynq PS. There are no hardware restrictions on how the memory is allocated or how it is shared between the two ARM cores.

3.5 Flash Memory

The design includes 64 MB of Quad SPI flash memory wired to the Zynq PS. This memory is available to the boot process. A 32 MB QSPI is wired to the Artix configuration pins.

3.6 MicroSD

A 3.3V Secure Digital micro card connector is wired to the PS and available to the boot process. A card detect pin is wired to the PS.

3.7 EEPROM

An M24C32 IIC EEPROM (4 kB) is available for board data. The EEPROM is wired to the Zynq PS and PL. A second part is wired to the Artix.

3.8 Clocks

The design includes a 33.3333 MHz oscillator from which all the PS clocks are derived.
It also includes a 10 MHz to 810 MHz VCXO wired to the PL clock that is programmable through I2C and a fixed 200 MHz oscillator. The 200 MHz is also wired to the Artix. Provision for a differential external PL clock is made through two SMC connectors.

3.9 GTX Transceivers

The design provides access to 16 GTX transceivers:
• Eight of the GTX transceivers are wired to the FMC HPC connector.
• One GTX transceiver is wired to the FMC LPC connector.
• One GTX transceiver is wired to the SFP/SFP+ Module connector (P2)
• One GTX transceiver is unused and is wired in a capacitively coupled TX-to-RX loopback configuration.

3.10 SFP

The design includes one small form-factor plugable (SFP/SFP+) connector and cage assembly that accepts SFP or SFP+ modules. It will support single or dual fiber or Ethernet SFP modules from the front panel. The SFP connector is wired according to specification SFP Transceiver 1.0 5/12/2001 snia.org SFFTA INF-8074i. Single transmit and receive differential pairs are wired to MGT ports. An MGT reference clock is wired to an IIC programmable oscillator. The current oscillator may have too much jitter for high speed SFP with current oscillator.
An 378928-B21-GT 1000BASE-T RJ-45 HP Blade System Compatible module was purchased for testing.

3.11 Ethernet

The design includes a Marvell Alaska Tri-Speed Ethernet PHY device for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports RGMII mode only. The front panel connection is through a RJ-45 connector with built-in magnetics and LEDs.

3.12 Front Panel

The Zynq VME Controller front panel includes LEDs indicating power status, FPGA DONE and a user LEDs. The user LED is wired to Zynq PS. The front panel has openings to expose the two FMC board panels. It also includes an SFP cage, an RJ45 socket wired to an Ethernet PHY, a USB micro B socket wired to a USB PHY, two USB-A sockets wired to RS232 interface chips and a RESET button.

3.13 FMC Connectors

The design includes one full LPC and one full HPC Vita Standard 57.1 FMC sockets. These include an I2C interface, 3.3V, 2.5V, 1.8V and 12V supplies. The HPC VADJ voltage is 2.5V. The LPC VADJ is 1.8V. The FMC faceplates are exposed to the front of card to allow external connections. The module PRESENT signals are wired to the PL. The CLK and CC FMC pins are wired to SRCC and MRCC

Zynq pins. The

3.14 Power

The six +5V VME power pins rated at 1.5 A per pin allows for 9.0 A or 45.0 W. This single slot VME supply power will restrict the applications that can be run on the Zynq VME Controller but based on measurements from the ZC706 this should not be a severe limitation. About 40 W would be available at 90 % regulator efficiency. Wiener specifies for the VME6000 crates 3.2 A per pin for a total of 19.0 A or 95 W. The ZC706 running an eight channel scope capture application accessing the 5 channel GPIO card and the FMC168 250 Msps ADC card draws 20.5 W steady state and 25.7 W peak. The Zynq PL is about 25 % utilized in this application. The Xilinx Vivado power estimate for this application is 3.0 W. The 4DSP FMC168 is specified to consume 13.5 W typical. The 4DSP FMC112 is specified to consume 12.0 W typical. An MVME3100 requires 28 W. Six additional power/ground pairs are wired to spare VME pins. This could allow maximum utilization of XC7Z045 (45W x 2).
All power comes from the 5V pins in the VME connectors through a fuse. VME +12V is also wired to the FMC connectors through a fuse. The following supplies are generated on the board.

VCCPINT, 1.0V, 2.0A Max.
VCCPAUX, 1.8V, 2.0A Max.
VCC1V5PS, 1.5V, 4.0A Max.
VCC3V3PS, 3.3V, 4.0A Max.
VCCINT, 1.0V, 20A Max.
VCCINT_ARTIX, 1.0V, 4.0A Max.
VCCAUX, 1.8V, 10.0A, Max.
VCCAUX_ARTIX, 1.8V, 2.0A Max.
VCCAUX_IO, 2.0V, 3.0A Max.
VADJ, 2.5V, 6.0A, Max.
VCC3V3, 3.3V, 10.0A Max.

VTTREF_PS, 0.75V, NA
VTTDDR_PS, 0.75V, 4.5A Max.

MGTVCCAUX, 1.8V, 3.0A Max.
MGTAVCC, 1.0V, 3.0A Max.
MGTAVCTT, 1.2V, 3.0A Max.

"Power Good" from each regulator enables next regulator in a fixed power up sequence. The sequencers hold the PS reset until all supplies are good. The Zynq supplies are monitored internally. Voltage and current for the high current supplies are also monitored by XADC through an FET mux into the Zynq. The sequencers are set for 10% tolerance and will attempt reverse sequence power down in the case of a drop in voltage.

3.15 Real Time Clock

The design includes an Epson real time clock chip with battery back up connected to the Zynq PS on an I2C bus. Its 32 Khz clock and its interrupt line are wired to the Zynq.

3.16 ADCs

The Zynq XADC will be used to monitor all on-board supply voltages and temperature.
It consists of two 12-bit x 1 MSPS ADC. Two channels will be connected through op-amps to SMCs. The XADCs will use an external 1.25V reference.

3.17 Zynq IIC

An IIC mux connects the ZYNQ to multiple IIC devices. The bus can be accessed from PS or PL. The devices are FMC HPC, FMC LPC, RTC, programmable oscillator to the Zynq PL, programmable oscillatorto the SFP and the EEPROM.

4. Configuration

Switches select whether to boot the Zynq from JTAG, QSPI or micro SD card. MIO[7] and MIO[8] are pulled up indicating the MIO banks are at 1.8V. MIO[6] is pulled up indicating setting the PS_PLL for wide range.

5. Reset

The Zynq PS reset is driven by the VME_SYSRESET, JTAG resets, loss of VCC5V, VCC3V3_PS or VCCP1V8 or a push button. A MAX16025 guarantees minimum length reset pulse. Zynq power on reset is driven by any supply out of range as monitored by power sequencers or a push button.

6. Debug

Three JTAG headers are provided to support the Xilinx debug tools. The Zynq PL and the Artix FPGA are on their own JTAG chains. The Zynq PS JTAG chain includes the FMC cards with FET bypass switches.

7. Environmental

Temperature
Operating: 0°C to +45°C
Storage: –25°C to +60°C
Humidity: 10% to 90% non-condensing
Zynq requires a heat sink.

8. Mechanical

The ZC706 board has a 16 later stack-up with parts on the top and bottom, four inner signal, four power and six ground layers. It includes buried vias. The Zynq VME Controller design is of comparable complexity and area. The design requires many impedance controlled and length matched differential traces. The number of layers will be set by maximum VME board thickness spec (0.063 +/- 0.008”). (ZC706: 10.5” x 5.5” x 0.059 (57.75) (MVME3100 9.2” x 6.3” x 0.063” x 0.8” (57.96).

9. Manufacture and Testing

A significant software development effort will be required to verify the design on the first run of boards and to provide a thorough self test capability. A VME standard qualification may also be required or at least compatibility with a selection of the existing custom boards needs to be verified.

10. Notes

The design will be compatible with the utility module, delay module and other BNL VME cards.
The design allows reuse of Xilinx Linux drivers and tools from Xilinx eval boards.

11. TTD

BOM needs to be completed. Design unlikely to fit in board space. Some pairing of features required.

12. Bill of Materials for Cost Estimate

Description	Manufacturer	Part Number	Quantity	Package	Supply	Cost
VME buffer	Texas Instruments	SN74VMEH22501DGGR	10		3.3 V	45.2
VME Connector	EPT	02 01 160 2101	2	96 Pin		15.4
VME Controller FPGA	Xilinx	XC6SLX9-2FTG256C	1		3.3, 1.2 V	19.0
SFP Cage	Molex	74754-0101	1			5.6
SFP Connector	Molex	74441-0010	1			3.0
USB Phy	SMSC	USB3320C-EZK-TR	1			1.8
Multiplexer	Analog	ADG707BRUZ	1		2.5 V	6.4
EEPROM	ST Micro	M24C08-WDW6TP	1		2.5 V	0.1
PS Oscillator	SiTime	SIT8103AC-23-18E-33.33333	1		2.5 V	????
Ethernet PHY	Marvell	88E1116R	1		3.3 V	????
Real Time Clock	Epson	RTC-8564JE	1		3.3 V	3.8
Rechargeable Battery	Panasonic	ML-621S/DN	1		3.0 V	2.1
USB UART Bridge	Silicon Labs	CP2103GM	1		3.3 V	3.7
SPI Flash	Spansion	S25FL128S	4		3.3, 2.5 V	14.4
FPGA	Xilinx	XC7Z045-2FFG900C	1		3.3, 2.5, 1.8, 1.5 V	2100.0
PL Oscillator	Silicon Labs	570BAB000544DG	1		2.5 V	35.0
SODIMM Cage	Leader Tech	20S-CBSFNSV-1.50X3.0X0.35	1			????
PS SDRAM	Micron	MT8JTF12864HZ-1G6G1	1		3.3, 1.5 V	87.2
PL SDRAM	Micron	MT41J256M8HX_15E	4		3.3, 1.5 V	????
FMC Connector	Samtec	ASP-134603-01	2			25.4
Micro SD Connector	Molex	504570-0893	1			????
Regulator	Texas Instruments	LMZ31520	1			18.3
Regulator	Texas Instruments	LMZ31710	2			18.6
Regulator	Texas Instruments	LMZ31506	2			18.6
Regulator	Texas Instruments	TPS79433DCQR	2			3.5
Voltage Reference	Texas Instruments	REF3012AIDBZT	1			1.5
Current Sensor						
16 Layer PCB		233 x 160 mm x 9.2 x 6.3 x .062 inches	1			300.0 160.0

Description	Manufacturer	Part Number	Quantity	Package	Supply	Cost
VME buffer	Texas Instruments	SN74VMEH22501DGGR	10		3.3 V	45.2
Heat sink/fan						
Faceplate			1			40.0
						3200