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ITS upgrade

RUv2 manual

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Document History

Version	Date	Author	Section	Description
0.1	31-October-2018	M.J. Rossewij	-	First concept.

Contents

1 Connectors

The table below gives an overview of the RUv1 connectors. More details are presented in the following subsections.

CONNECTORs		Type	Function/Intended for
J0	POWER	MOLEX172316-xx04	Front panel power-in for table top operation
J1	VME J1 style	DIN41612	Power-in for rack operation & alternative Power board control
J2 J24	Transition Board	2 * ERF8-050-05.0-L-DV	Interface to Alpide sensor modules via transition board
J3	VTRx	TYCO 1888247	Primary (sensor) data uplink & control/status link
J4	VTTx		Up to 2 optional (sensor) data uplinks
J5	VTRx		Downlink for receiving trigger/timing
J6	USB3	micro B SuperSpeed	USB3 connector for table top operation
J7	BUSY_AUX	ERF8-010-01-L-D-RA-L	BUSY signal and optional links for future applications
J8	JTAG	MOLEX_08783-1420	Programming FPGAs (compatible with Xilinx 20 pin connector)
J9	CAN	RUv2_0: Molex87833-0420 RUv2_1: Molex87833-0620	Access in absence of DAQ/GBT system
J10	Power mezzanine Board	ERF8-030-05.0-L-DV-TR	Primary path for Power board control & LEDs
J11	JTAG	HTST-105-01-L-DV-A	Programming FPGAs (compatible with Microsemi connector)
J12	GBTx I2C interface	Boxed header 4x2	Access to GBTx registers using CERN USB-I2C dongle
TEST-CONNECTORs			
J13	Xilinx pinheader	TSM-110-04-T-DV	Connected to Bank47 (1,8V)
J14	PA3 pinheader		Connected to Bank 5 (3,3V)
J15	JitterCleaner_IN+	SMA	Alternative/external input for jitter cleaner or output for monitoring U18 output 8
J16	JitterCleaner_IN -		
J17	clockBuffer_IN+		Alternative/external input for 1-8 LVDS primary clock buffer (U18)
J18	clockBuffer_IN -		
J19	clockBuffer_OUT -		1-8 LVDS secondary clock buffer (U17) output 4
J20	clockBuffer_OUT+		
J21	XilinxIO -		Xilinx bank 68 (1V8) differential test IO
J22	XilinxIO+		
J23	FAN connector	MOLEX-22-11-2032	FAN power connector

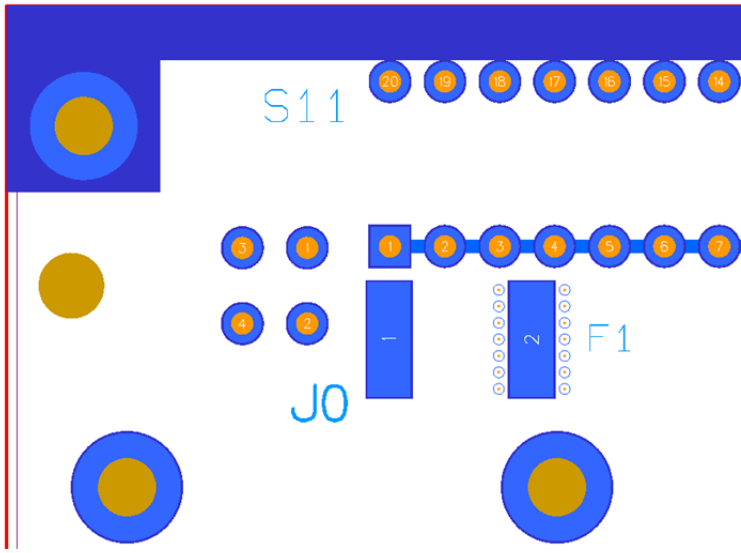
1.1 J0, Power connector

For table top operation, Power can be applied on the J0. Voltage can range from 5…12V. Take into account voltage drop on power leads to ensure the actual input voltage is ≥5V. Also take care that the voltage applied is compatible with the FAN connected to J23. Typical settings:

Voltage (V)	Typical Current (A)
5	3
12	1,5

J0 pinnout:

Pin	Function
1,2	Power_In
3,4	GND



J1 VME style

The type and position of the J1 connector is compatible with the VME standard, including the location of the (GND, 5 & 12V) power pins. When using J1 for powering, the placement of the polyswitch-fuses determines which J1 power input is used:

Voltage (V)	Current (A)	F2	F3
5	3	PolySwitch 5A 2920L500/16MR	Absent
12 (DEFAULT)	1,5	Absent	PolySwitch 2A2 2920L200DR

REMARK: Do not place both Polyswitch fuses (F2&F3) as this results into a short
Also here, take care that the voltage selected is compatible with the FAN connected to J23.

The complete J1 pinout is shown below:

	VME-J1				**J1 backplane**		
	Row A	Row B	Row C		Row A	Row B	Row C
1.	D00	BBSY	D08				INFGND
2.	D01	BCLR	D09				INFGND
3.	D02	ACFAIL	D10				
4.	D03	BG0IN	D11				
5.	D04	BG0OUT	D12				
6.	D05	BG1IN	D13				
7.	D06	BG1OUT	D14				
8.	D07	BG2IN	D15				
9.	GND	BG2OUT	GND		GND		GND
10.	SYSCLK	BG3IN	SYSFAIL				
11.	GND	BG3OUT	BERR		GND		
12.	DS1	BR0	SYSRESET				
13.	DS0	BR1	LWORD				
14.	WRITE	BR2	AM5				
15.	GND	BR3	A23		GND		
16.	DTACK	AM0	A22				
17.	GND	AM1	A21		GND		
18.	AS	AM2	A20				
19.	GND	AM3	A19		GND		
20.	IACK	GND	A18			GND	
21.	IACKIN	SERCLK	A17				
22.	IACKOUT	SERDAT	A16				
23.	AM4	GND	A15			GND	
24.	A07	IRQ7	A14				
25.	A06	IRQ6	A13				
26.	A05	IRQ5	A12				
27.	A04	IRQ4	A11				
28.	A03	IRQ3	A10				
29.	A02	IRQ2	A09				
30.	A01	IRQ1	A08				
31.	-12 V	+5 V STDBY	+12 V				+12V
32.	+ 5 V	+5 V	+5 V		+5V	+5V	+5V

1.2 J2 Transition board

After inserting the transition board in J2&J24, it can be fixated with 4 M2 bolt/nuts. The J2/J24 pinout can be found in the schematics. Depending on the decoupling capacitors placed, ALPIDE_DATA_MGT_dp[27] shares a MGT with BUSY_IN (for more details, see section 1.7).

1.3 J3 VTRx

J3 allows the installation of a VTRx to provide the primary GBT transceiver path for data and control. The VTRx should be fixated with 2 M1.4 screws.

1.4 J4 VTTx

J4 allows the installation of a VTTx to provide up to 2 additional GBT uplink data channels. The VTTx should be fixated with 2 M1.4 screws.

1.5 J5 VTRx (single mode)

J5 allows the installation of a VTRx (-SingleMode) to provide a receive path for the trigger (and LHC bunch clock). The VTRx (-SingleMode) Tx channel is unconnected and the Rx channel is connected with GBTx2. The VTTx (-SingleMode) should be fixated with 2 M1.4 screws.

1.6 J6 Micro B USB3

J6 is a Micro B USB3 (super speed) receptable, intended for table top operation and/or when no GBT/DAQ system is available.

1.7 J7 BUSY-AUX connector

The BUSY_AUX connector has the following pinout:

pin	Signal	Pin	signal
1	GND	2	GND
3	BUSY_IN_P	4	BUSY_OUT_P
5	BUSY_IN_N	6	BUSY_OUT_N
7	GND	8	GND
9	AUX_dp0	10	AUX_dp1
11	AUX_dn0	12	AUX_dn1
13	GND	14	GND
15	AUX_dp2	16	AUX_dp3
17	AUX_dn2	18	AUX_dn3
19	GND	20	GND

The BUSY_OUT signal goes to the Xilinx US MGT27 transmitter and the BUSY_IN goes to the Xilinx US MGT27 receiver. The receiver is shared with the 27th sensor receiver pair. The connectivity of the MGT27 receiver is selected by placing/removing the proper capacitors:

MGT27 receiver function	C319&C320	C526/C530
ALPIDE_DATA_MGT_27	Removed	Placed
BUSY_IN	Placed	Removed
Default (bad SI due to stubs)	Placed	Placed

The 4 AUX signals are connected to the Xilinx US FPGA select IO (e.g. LVDS) and routed as differential pairs. The direction (IN/OUT/BI) is determined by the firmware. These signals are intended for optional future use.

1.8 J8 JTAG connector (front panel)

The front panel JTAG connector is compatible with the Xilinx 20 pin connector. The SCA-JTAG, J8 and J10 can act as JTAG masters and are connected in parallel. Placing the Xilinx download cable automatically disconnects (using PGND to disable U19, the FET switch) the SCA JTAG master from the JTAG chain.

1.9 J9 CAN connector

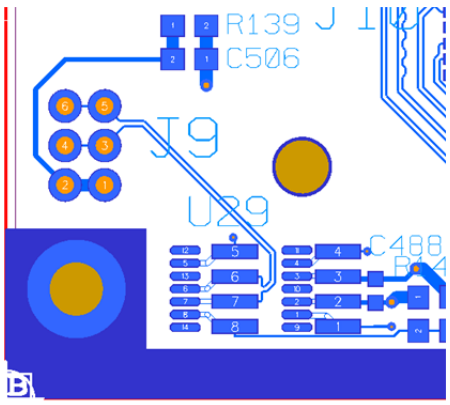
This CAN is intended to provide an alternative path to access the RU and Power board when the GBT/DAQ system is not available. The CAN connector has the following pinout:

Below: RUv2_0 pinout

pin	Signal	Pin	signal
1	CANL	2	GND
3	CANH	4	GND

pin	Signal	Pin	signal
1	GND	2	GND
3	CANL	4	CANL
5	CANH	6	CANH

Above: RUv2_1 pinout: This allows more easy front panel chaining of the CAN signals



There is no CAN bus termination on the RU.

1.10 J10 Power mezzanine

The main function of the power mezzanine is to provide the primary access path to the power board using several I2C busses. The power mezzanine also has 6 LEDS: LED[0:3] are connected to the Xilinx US FPGA and LED[4:5] go to the Microsemi PA3 FPGA. The power mezzanine can be fixated using 2 M2.5 bolts/nuts. The J10 pinout can be found in the schematics.

1.11 J11 JTAG connector (Microsemi-FlashPro compatible)

J11 allows direct connection of the microsemi FlashPro(4) download cable. When connecting the download-cable, the SCA-JTAG master is automatically disconnected (by disabling U19, the FET switch) from the JTAG chain. Jumper J11 also disables U19 (and disconnects the SCA-JTAG) and provides improved GND connection to the FlasPro download cable.

1.12 J12 GBTx I2C connector

J12 provides a path to access and program the GBTx with the Cern configuration software by connecting the CERN USB-I2C dongle. To access to the GBTx from the dongle, the Xilinx I2C master and the SCA I2C [7] master must be disabled. All 3 GBTx share the same I2C bus:

device	Address	FusePower	FusePulse
GBTx	0x1	R279	R280
GBTX1	0x3	R282	R283
GBTX2	0x5	R285	R286

If needed, individual resistors (shown above) can be placed/removed to provide the FusePower and FusePulse to an individual GBTx during the fusing process.

1.13 J13 Xilinx GPIO header

Provides access to 10 signals from Xilinx bank 47 (1,8V).

1.14 J14 PA3 GPIO header

Provides access to 10 signals from PA3 Bank 5 (3,3V).

1.15 J15 & J16 Jitter Cleaner SMA differential input

To provide an external clock signal to the jitter cleaner. Intended for test purposes. Selection of the jitter cleaner input source is done by S10_A1 or CS signal (coming form PA3):

S10[1]	R162	CS	Jitter Cleaner source
0	NP	X	GBTx Clockdes6
T	0	0	
T	0	1	primary clock buffer output 8
1	NP	X	or SMAJ15/J16 In

Furthermore resistors or capacitors must be placed on J34 and J35 in such a way that the SMA signal is propagated to the jitter cleaner. Alternatively, J34 & J35 can also be placed to provide a path for monitoring the primary clock buffer output 8.

1.16 17 & J18 Primary clock buffer (U18) input

External test-input for the primary clockbuffer (U18). By default (=pulldown R214 placed, pullup R215 removed), U18 uses the 160.31588 MHz Xtal oscillator. To use/enable this SMA test input, place pull up R215 (and remove R214).

1.17 J19 & J20 Secondary Clock Buffer (U17) SMA differential output

Secondary Clock buffer LVDS monitoring output U17-4. Source of U17 can be selected with the IN_SEL signal coming from the PA3 (with R218 placed) or with R213/R219 pull-up/down resistors. Pulldown (defaults) selects primary clock buffer output, pull up the jitter cleaner output.

1.18 J23 Fan Connector

The Fan connector pinout is:

Pin	RUv1.1
1	GND
2	PowerIn (=J0 or J1-5V(12V) when F2(F3) placed)
3	NC

2 Jumpers

The table below gives an overview of the RUv1 jumpers:

RefDes	Function	Default
J28	GBTx2 configSelect	2-3 (1V5, I2C)
J29	GBTx configSelect	1-2 (GND, IC channel)
J30	JTAG bypass PA3	1-2 (include)
J31	JTAG bypass Xilinx	1-2 (include)
J32	Disconnect SCA-JTAG & extra GND FlashPro cable	Not placed
J33	Enable DONE and INIT_B LED	Not placed
J34	SMA to primary clk buffer output or Jittercleaner input	Jittercleaner input
J35		

Default refers to the setting during the actual Alice experiment.

2.1 J30 JTAG bypass PA3

J33 includes (or bypasses) the PA3 in the JTAG chain. The PA3 JTAG provides besides boundry scan also the FPGA configuration interface. It is foreseen to be the primary path to reprogram the PA3 (from the SCA JTAG master) when the system is installed. Therefore the default configuration is to include the PA3 in the chain.

2.2 J31 JTAG bypass Xilinx

J34 includes (or bypasses) the Xilinx in the JTAG chain. The Xilinx JTAG provides besides boundry scan also access to the FPGA configuration logic. As this provides a path for scrubbing actions, the Xilinx JTAG is included in primary JTAG chain in the default configuration.

2.3 J32 Disconnect SCA-JTAG & extra GND FlashPro cable

Placing J39 disables the FET switch (U19: QS3VH126S1G) which disconnects the SCA JTAG master from the JTAG chain. In addition, it provides an improved GND connection to the FlashPro cable. As the SCA-JTAG master is intended for accessing the FPGA configuration when the system is installed, the jumper should not be placed in the default configuration.

2.4 J33 POWER to DONE and INIT_B LED

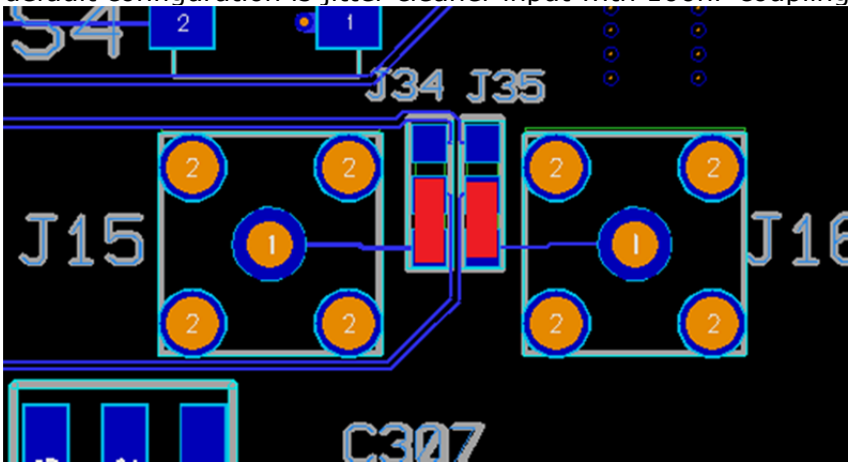
J40 enables or disables the bicolored LED D2 which indicates the status of the INIT signal. As no light sources are allowed in the magnet during the experiment, the jumper must not be placed in the default configuration.

2.5 J28 & J29: GBTx2 & GBTx0 configSelect

J28 & J29 select whether the GBTx2 & GBTx0 are configured via the IC channel (optical link) or the GBTx I2C interface (using the Cern USB-I2C dongle or the Xilinx FPGA as I2C master). In the default configuration, GBTx is set to the IC channel (allowing it to be controlled directly from the control room GBT link) while GBTx2 are controlled via I2C. GBTx1 is hardwired to I2C control.

2.6 J34 & J35 SMA to JitterCleaner_CLKIN1 or primary clock buffer out 4

These are not pin-header jumpers but SMA resistor/capacitor selection circuits allowing SMA J15 & J16 to be connected to the JitterCleaner CLKIN1 input or the primary clock buffer (U18) output 4. The default configuration is jitter cleaner input with 100nF coupling as shown below:



3 Switches

The RU has the following switches

S0…S3	Push button connected to both PA3 and Xilinx Pushed =>HIGH (1V8) Relaxed => LOW (GND)
S4	Push button: Reset Jitter Cleaner (U28: Si5316)
S5	Push button: Reset GBTx, GBTx1 GBTx2 and SCA
S6	Push Button: Reset FX3 (U5: CYUSB3014)
S9	DIP switch for FX3 configuration (see below)
S10	DIP switch for jitter cleaner configuration (see below)
S11	10 channel DIP switch connected to both PA3 and Xilinx ON position => High (1V8) OFF position => LOW (GND) Intended for testing purposed or to set a CAN bus address

3.1 S9 FX3 configuration

S9 is an 8 channel DIP switch. Each channel has 3 states:

1. +: HIGH, pulled to 1V8
2. 0: Floating
3. -: LOW, pulled to GND

S9 channel	Function	Default
1	PMODE[0]	F (I2C, On failure USB Boot is enabled)
2	PMODE[1]	1
3	PMODE[2]	F
4 – 8	Unused	X

PMODE selects the FX3 boot source:

PMODE[2:0]	Boot from
F11	USB boot
F1F	I2C, On failure USB Boot is enabled
1FF	I2C only

3.2 S10 JitterCleaner configuration

S10 is an 8 channel DIP switch. Each channel has 3 states:

1. +: High, pulled to VSI (2,5 or 3,3V)
2. 0: Middle/Floating
3. -: Low, pulled to GND

S10 channel	Name	Function	Default
1	CS	Clock Select	
2	DBL_BY	Output disable/bypass	
3	SFOUT[0]	Signal Format Select	M
4	SFOUT[1]		H
5	FRQSEL[0]	Frequency select	L
6	FRQSEL[1]		M
7	BWSEL[0]	PLL bandwidth Select	TBD
8	BWSEL[1]		TBD

CS: Clock Select

L	CLKIN1: SMA J15/J16
M	Selection controlled by PA3 (if R162 placed)
H	CLKIN2: GBTx CLOCKDES6

DBL_BY: Output disable/bypass

L	CKOUT enabled
M	CKOUT disabled
H	Bypass mode with CKOUT enabled

SFOUTn: Signal Format Select

HM	LVDS
HL	CML

MH	LVPECL
ML	Low Swing LVDS
LH	CMOS
LM	Disabled
others	Reserved

FRQSEL: Frequency select

FREQSEL[1:0]	F_{MIN}(MHz)	F_{MAX}(MHz)
LL	19.38	22.28
LM	38,75	44.56
LH	77.5	89.13
ML	155	178.25
MM	310	356.5
MH	620	710

The optimal PLL bandwidth Select (BWSEL) needs to be determined experimentally.

4 LED

The RUv1.0 has two bi-colored LED (D2) indicating the XILINX FPGA INIT_B and DONE signals status:

5 Xilinx

The Xilinx has the following bank:

Bank	Voltage	Interface/functioin
0	1,5V	Configuration/Slave SelectMap
44	GND	Unused
45	1V8	FX3 interface (DQ[0:31], CTL[0:12], INT_n, CLK, RESET, UART_RX/TX)
46	1V8	GBTx SLVS (DIN[0:9], DOUT[0:9], DCLK[0:1])
47	1V8	GBTx1 SLVS (DIN[0:9]) GBTx CLOCKDES[2:3] LOCALCLK[2] AUX[0:3] differential signals LED[0:3] GPIO PINHEADER
48	1V8	GBTx2 SLVS (DIN[0:9], DOUT[0:9], DCLK[0:1]) PUSHBUTTON[0:3]
64	3V3	Alpide Sensor Control Interface (DCLK[0:5], DCTRL[0:5]) Power Board Interface (SCL1/2_(AUX)_READ/WRITE, SDA1/2_(AUX)_READ/WRITE,)
65	1V5	Slave SelectMap
66	1V8	Alpide Sensor Datal Interface (ALPIDE_DATA_GPIO[1:24])
67	1V5	GBTx/1/2 CMOS signals (TXRDY, RXRDY, RXDATAVALID, TXDATAVALID) I2C master to GBTx1/2 SCA (GPIO[0:11], I2C4 slave, SPI slave)
68	1V8	Alpide Sensor Datal Interface (ALPIDE_DATA_GPIO[0], ALPIDE_DATA_GPIO[25:27]) DIPSWITCH[0:9] PA3 single ended IO (PA3_IO[0:11]) PA3 diff. out (PA3_IO_d[0:4]) PA3 diff. in (PA3_IO_d[5:9])

6 PA3

The PA3 (A3PE600L-FG484M) has the following banks:

Bank	Voltage	Interface/function
0	1V8	PA3 single ended IO (PA3_IO[0:11]) DIPSWITCH[0:9] PUSHBUTTON[0:3] LED[4:5]
1	1V5	Xilinx SelectMap (D[0:7], CCLK, CSI_B, DONE, INIT, PROGRAM, RDWR)
2	GND	Unused
3	GND	Unused
4	VSI	Jitter Cleaner Control signals (C1B, C2B, LOL, CS, RST)

5	3V3	Flash (DATA[0:7], CONTROL) CAN (D, R, LBK, RS) WATCHDOG/POWERON reset
6	1V5	SCA (GPIO[12:19], I2C0 slave, I2C5 slave)
7	2V5	Xilinx diff. in (FPGA_IN_d[0:4]) Xilinx diff. out (FPGA_OUT_d[5:9]) Clock input (CLOCKDES5, LOCAL_CLK) Clock Selection signal (IN_SEL) for Clock Buffer (U17:CDCLVD1212)

VSI is determined by the placement of L25 (2V5).

7 SCA

The SCA has a number of analog and digital (LVCMOS1V5) interfaces that are described here.

7.1 I2C

The SCA has 16 I2C masters, from which 7 are used on RUv1:

I2C	Connected to	Function
0	PA3	TBD
1	VTTx	Adjust 1st channel laser diode power
2	VTTx	Adjust 2nd channel laser diode power
3	VTRx2	Adjust laser diode power
4	Xilinx US	TBD
5	PA3	TBD
6	-	-
7	GBTx	Acces5 to the GBTx, GBTx1 and GBTx2 registers
8	-	-
9	-	-
10	-	-
11	-	-
12	-	-
13	-	-
14	-	-
15	-	-

The I2C-channel 7 in fact has 3 masters:

1) I2C channel 7
2) I2C master on the Xilinx
3) USB-U2C dongle connected to header J2

It is the responsibility of the user to ensure only one master is active.

7.2 GPIO

The SCA has 32 GPIO, from which 23 are used on RUv1:

GPIO	Connected to	Function
0..3	Xilinx US	Each GPIO is connected with 3 Xilinx IO pins to provide TMR
4…11		TBD
12…19	PA3	TBD
20…22	-	-
23	PROGRAM_B	Xilinx US configuration status signals
24	DONE	
25	INIT_B	
26…31	-	-

7.3 JTAG

The SCA has one JTAG master that (depending on the board jumper settings) can be connected to the following slaves: Xilinx US, PA3, GBTx, GBTx1, GBTx2 and FX3.
It is intended to configure the FPGAs, especially the PA3.

In fact there are 3 JTAG-masters possible:

- Xilininx download cable via front panel connector (J8)
- Microsemi FlasPro download cable (J11)
- SCA-JTAG

The SCA JTAG is connected to the JTAG chain with a switch (U19) that automatically disconnects the SCA JTAG master from the chain when one of the download-cables is plugged in.

7.4 SPI

The SCA has one SPI master that is connected to the Xilinx US. It can function as a backup communication path to the SEM IP.

7.5 ADC

The SCA has 31 ADC inputs(12 bit, 0,0…1,0V), from which 18 are used on RUv1:

I2C	Connected to	Measured voltage means	Calculation
0	I_{MGT}	$I_{MGT}/5$	$I_{MGT}=5*ADC_{VAL}/4095$
1	I_{INT}	$I_{INT}/5$	$I_{INT}=5*ADC_{VAL}/4095$
2	I_{1V2}	$I_{1V2}/5$	$I_{1V2}=5*ADC_{VAL}/4095$
3	I_{1V5}	$I_{1V5}/5$	$I_{1V5}=5*ADC_{VAL}/4095$
4	I_{1V8}	$I_{1V8}/5$	$I_{1V8}=5*ADC_{VAL}/4095$
5	I_{2V5}	$I_{2V5}/5$	$I_{2V5}=5*ADC_{VAL}/4095$
6	I_{3V3}	$I_{3V3}/5$	$I_{3V3}=5*ADC_{VAL}/4095$
7	I_{IN}	$I_{IN}/5$	$I_{IN}=5*ADC_{VAL}/4095$
8	V_{MGT}	$V_{MGT}/2$	$V_{MGT}=2*ADC_{VAL}/4095$
9	V_{INT}	$V_{INT}/2$	$V_{INT}=2*ADC_{VAL}/4095$
10	V_{1V2}	$V_{1V2}/2$	$V_{1V2}=2*ADC_{VAL}/4095$
11	V_{1V5}	$V_{1V5}/2$	$V_{1V5}=2*ADC_{VAL}/4095$
12	V_{1V8}	$V_{1V8}/2$	$V_{1V8}=2*ADC_{VAL}/4095$
13	V_{2V5}	$V_{2V5}/5$	$V_{2V5}=5*ADC_{VAL}/4095$
14	V_{3V3}	$V_{3V3}/5$	$V_{3V3}=5*ADC_{VAL}/4095$
15	V_{IN}	$V_{IN}/21$	$V_{IN}=21*ADC_{VAL}/4095$
16	V_{RSSI1}	Receiver optical power of VTRx1	$I(A) = (2,5 - ((ADC_{VAL}/4095)*69/22))/4700$
17	V_{RSSI2}	Receiver optical power of VTRx2	$I(uA) = 532 - 0,163 * ADC_{VAL}$
18..22	-	-	
23	R361	PT1000-Xilinx	$T(°C) = ((10*ADC_{VAL}/4095)-1)*1000/3,85$ or $T(°C)=0,634286 * ADC_{VAL} - 259,74$
24	R360	PT1000-Regulators	
25..30	-	-	

7.5.1 Regulator Voltage and current

In RUv1_1, ADC Channel 0…7 are used to measure the 8 power rail currents. All power rails have an effective (combination of sense resistor, amplifier gain and voltage divider) current sense resistor of 0,2Ω.

ADC Channel 8…15 are used to measure the 8 power rail voltages. They are pre-scaled using a resistor divider as indicated in the table.

7.5.2 VTRx Optical power

From V_{RSSI}, The optical average photo current can be calculated with:
$V_{RSSI}=(VCC-I*R1)*R2/(R1+R2)$
Filling in: R1=4k7, R2=2k2 and VCC=2,5V:
$V_{RSSI}=0,8-1499*I$
Or;
$I = (2,5 - (V_{RSSI}*69/22))/4700$

7.5.3 Temperature

The PT1000 are 1 kΩ at 0 °C. The temperature sensitivity is 3850ppm/K, or 3,85Ω/K. so:
$R=1000+3,85*T$
Using the SCA-ADC channel internal (100μA) current source, the measured voltage corresponds to:
$U=I*R=0,0001(1000+3,85*T)$
So
$T=(10*U-1)*1000/3,85=(10.000*U-1000)/3,85$

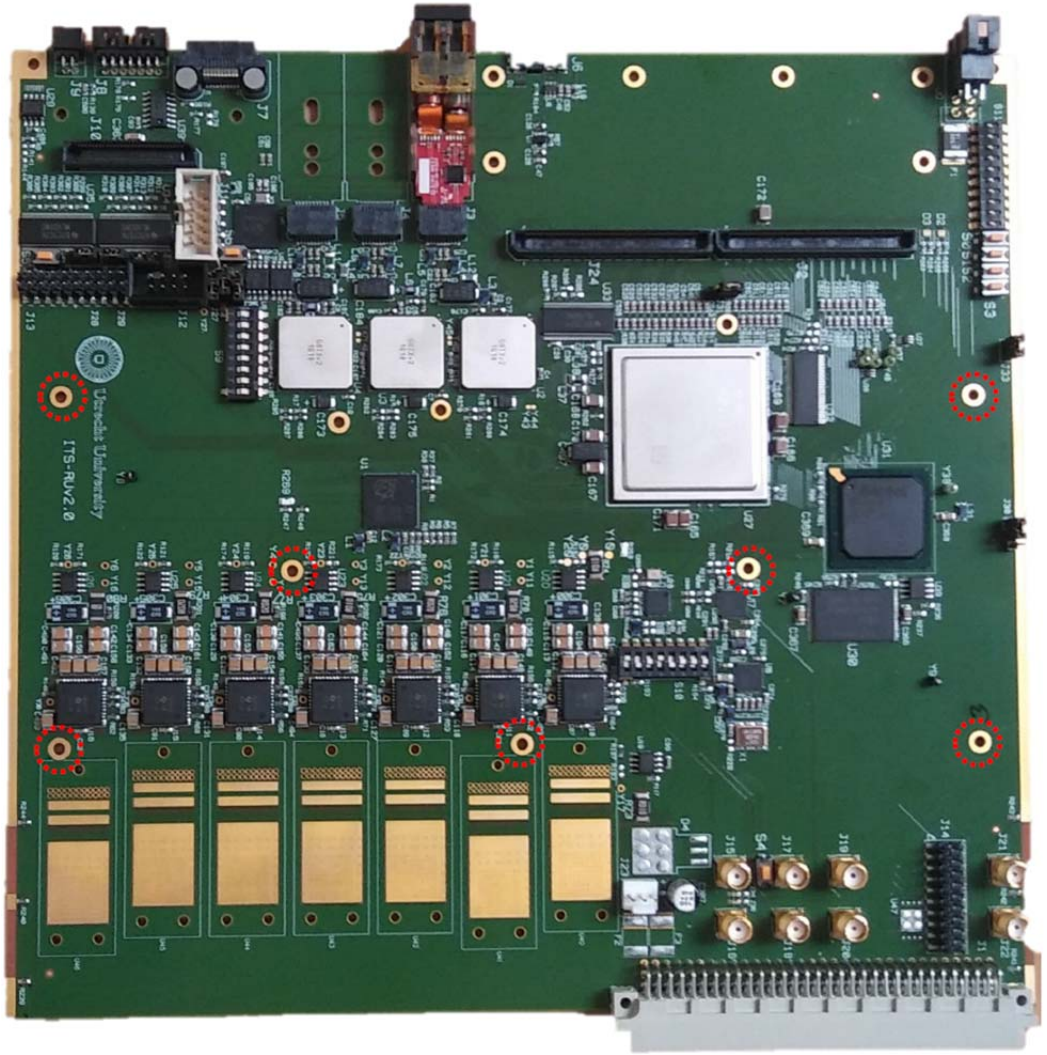
7.6 DAC

Not used

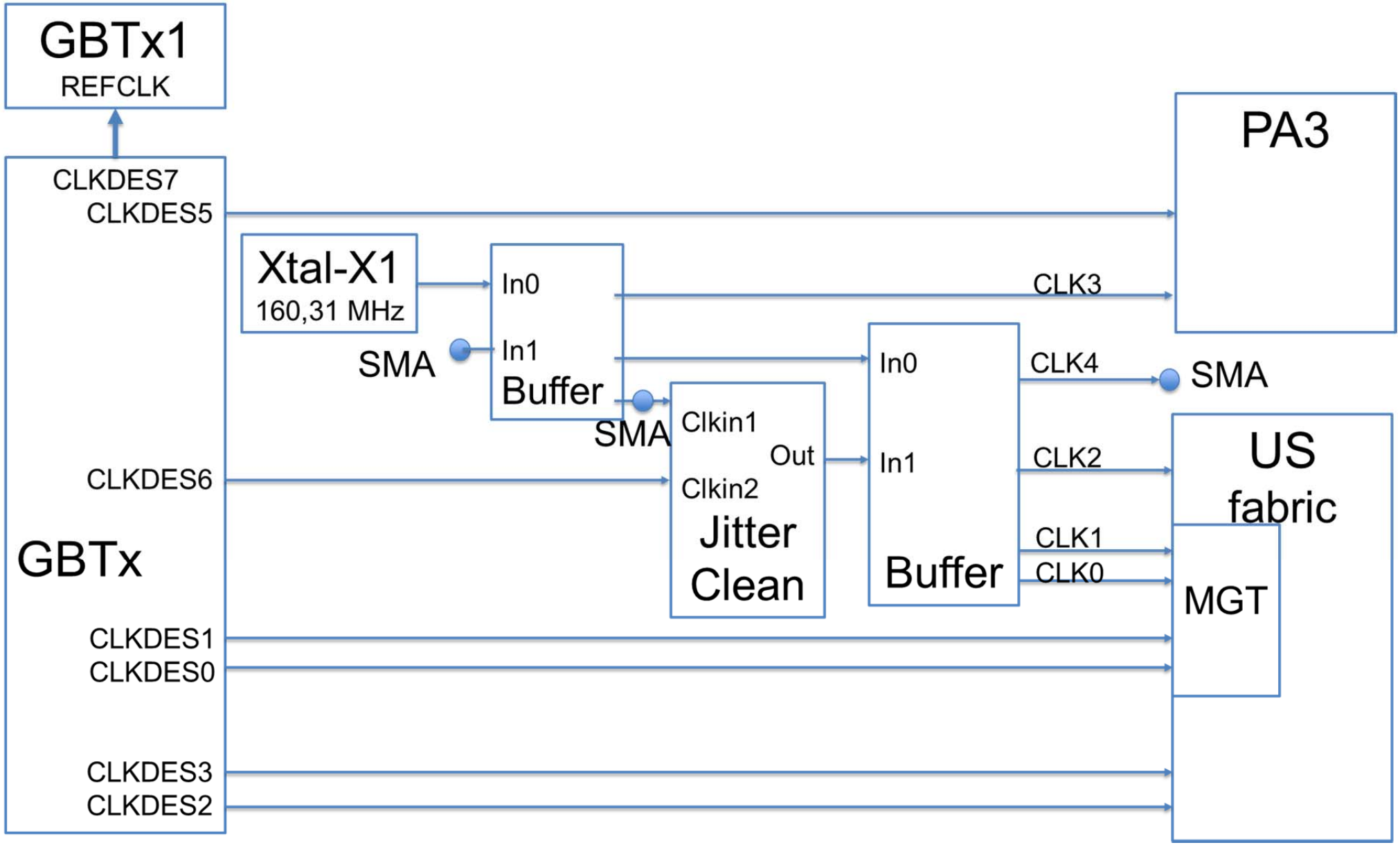
8 Differences RUv2_0 & RUv2_1

The following table shows the differences between RUv2_0 and RUv2_1:

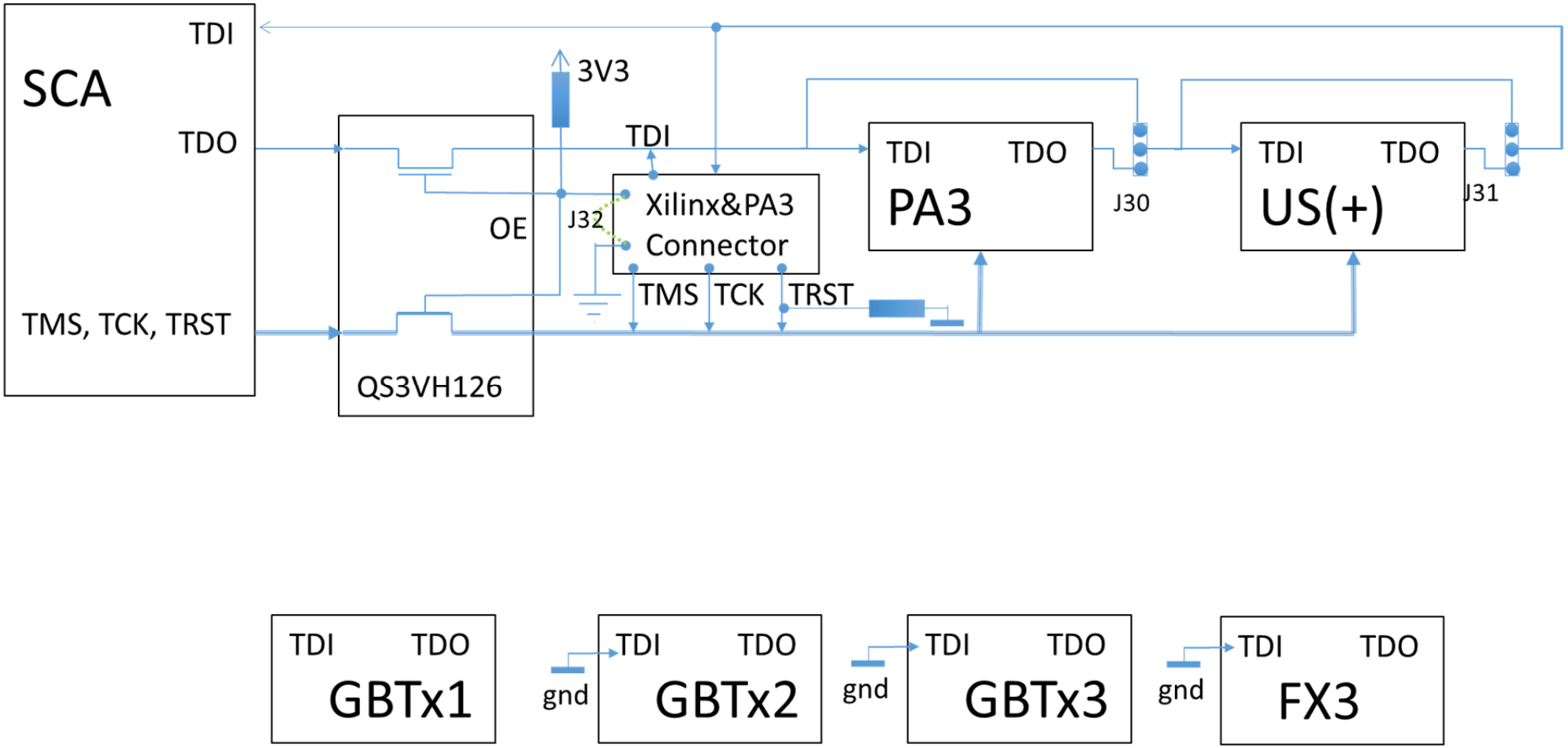
REFDES	Type	Sheet	RUv2_0	RUv2_1	Motivation
J9	Improvement	4	4 pin CAN connector Molex87833-0420	6 pin CAN connector Molex87833-0620	To ease the board to board front panel CAN signal cabling
	Fix		I_{IN} 20% too high	I_{IN} ok	Fixed I_{IN} sense resistor routing
			Y7-9 & Y37-42 placed	Not populated	Due to height constraints, test points under cold plate are not placed
	Improvement		Cold plate mounting Holes are for M2.5	Cold plate mounting Holes are for M3	To be compatible with the threads in the coldplate, the mounting (indicated below) holes are enlarged from M2.5 to M3



Appendix A : RUv2 clocking scheme



Appendix B RUv1 JTAG configuration scheme



Appendix C RUv1 Block Diagram