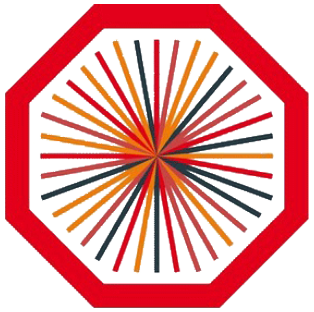
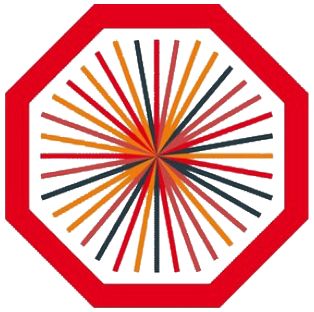
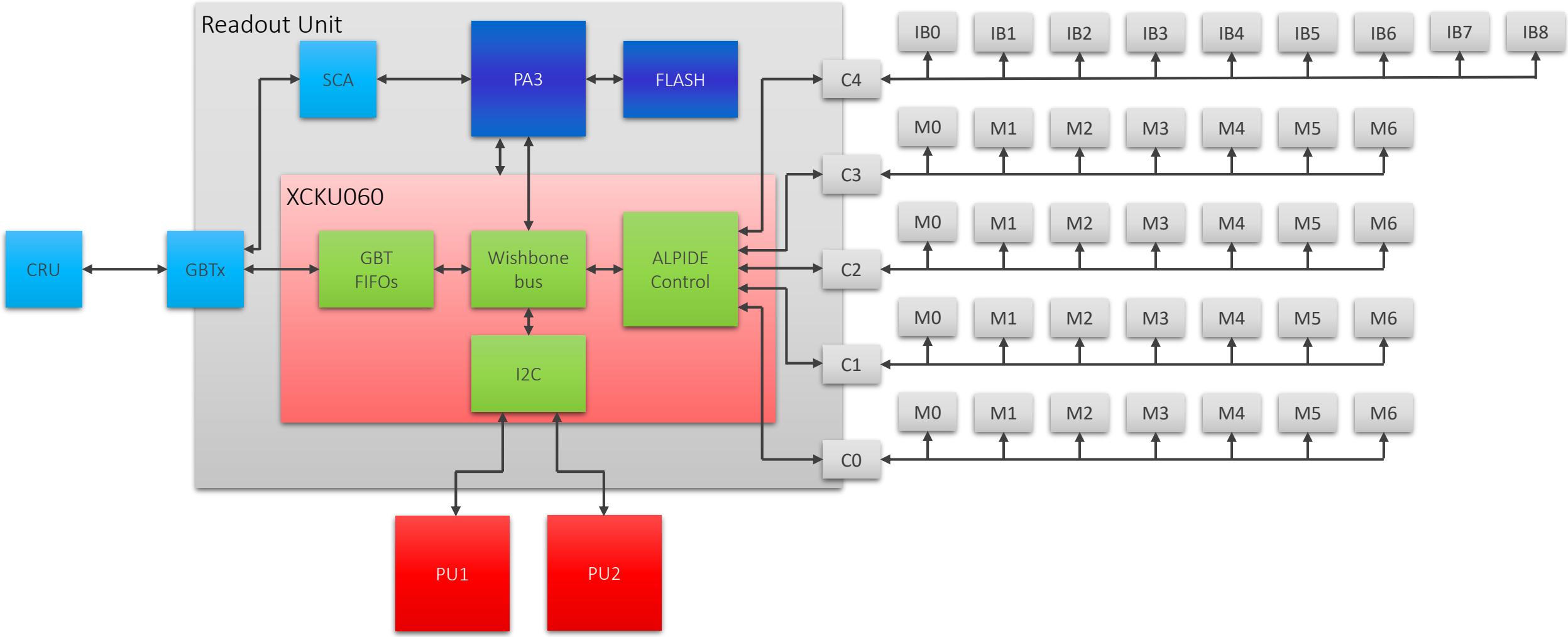
ALICE



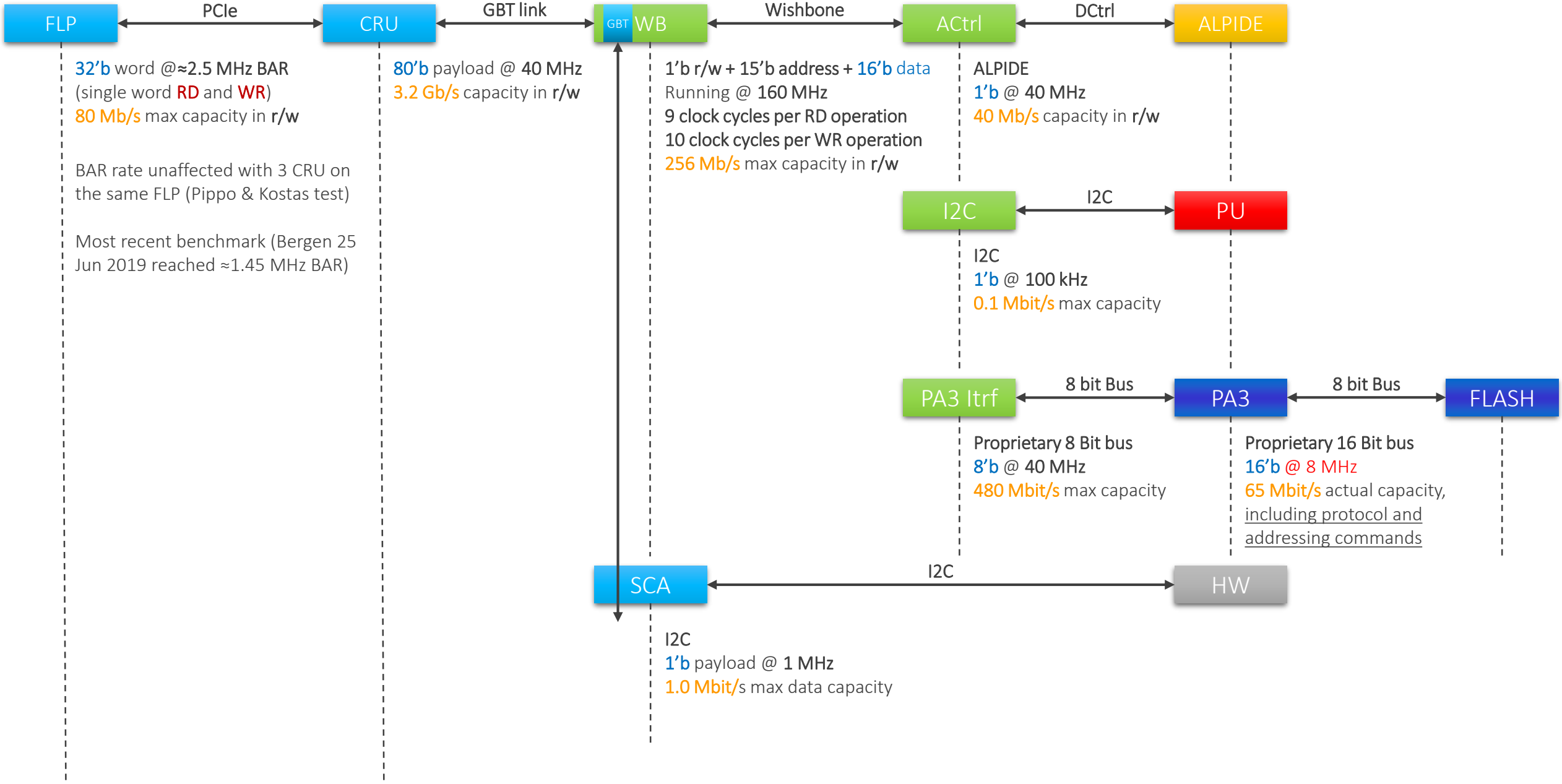
ITS Slow Control



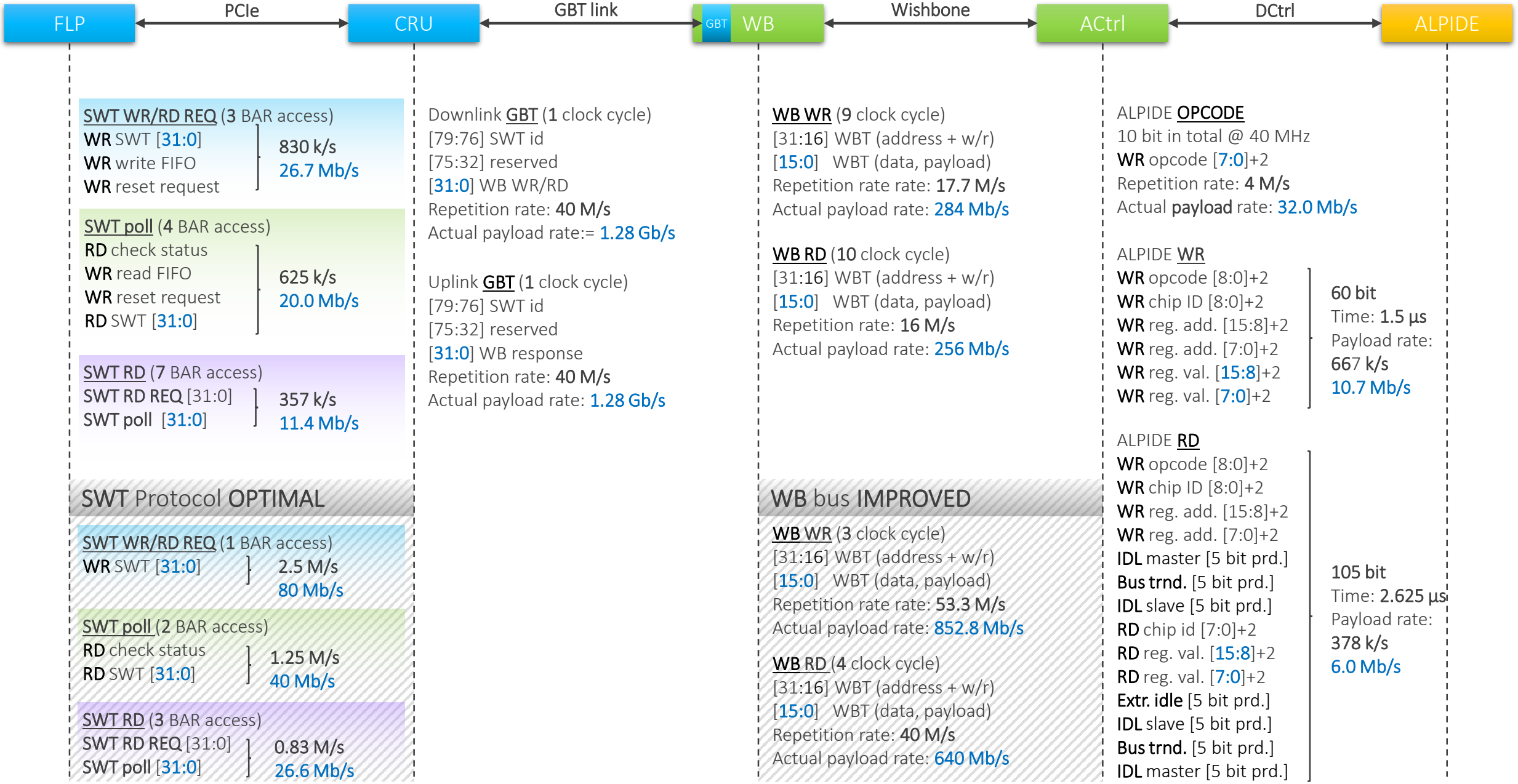
ITS readout slow control actual implementation


Readout Unit
SCA
PA3
FLASH
XCKU060
CRU
GBTx
GBT FIFOs
Wishbone bus
ALPIDE Control
I2C
PU1
PU2
C4
C3
C2
C1
C0
IB0
IB1
IB2
IB3
IB4
IB5
IB6
IB7
IB8
M0
M1
M2
M3
M4
M5
M6

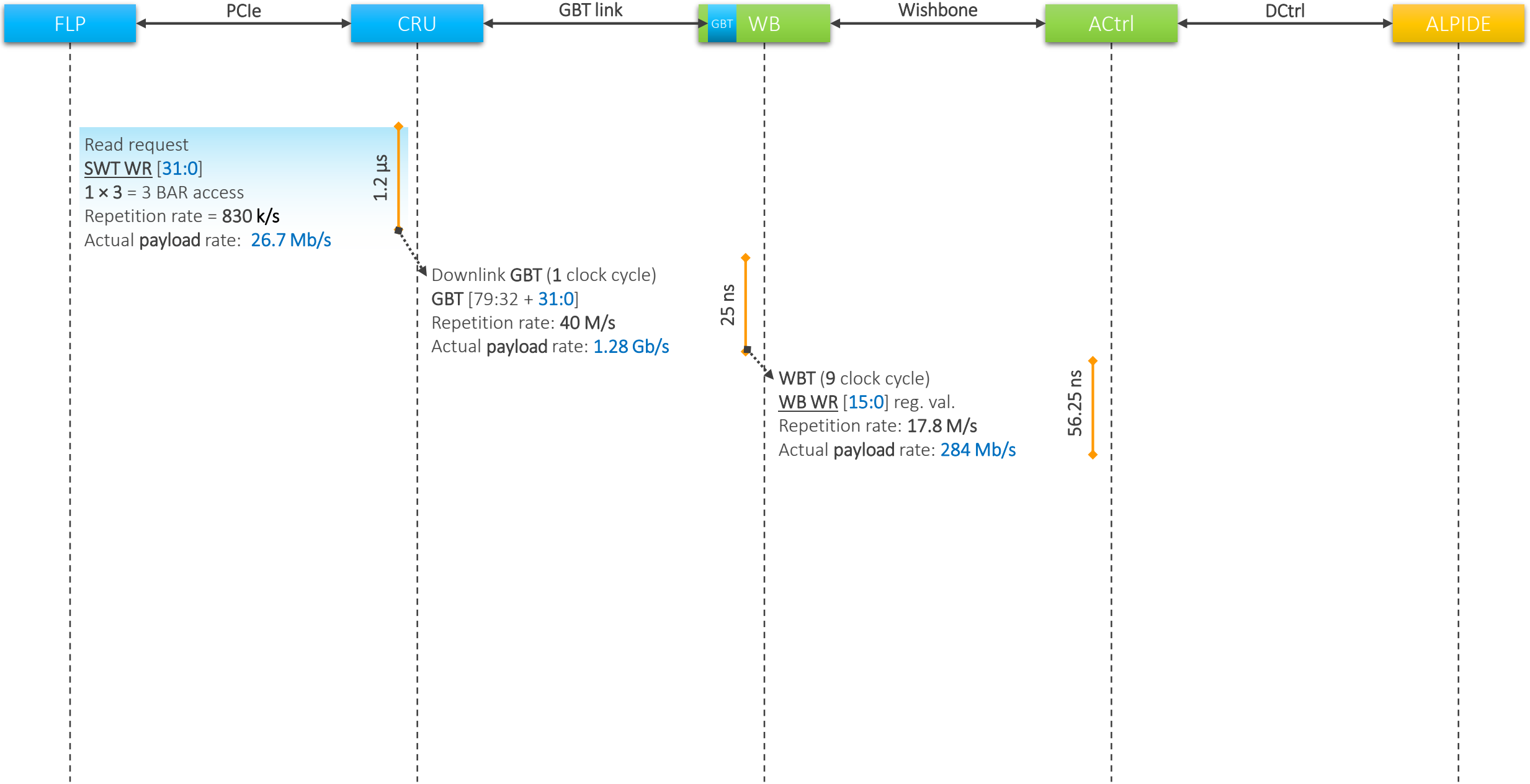
Physical transfer layers overview – maximum theoretical payload and capacity



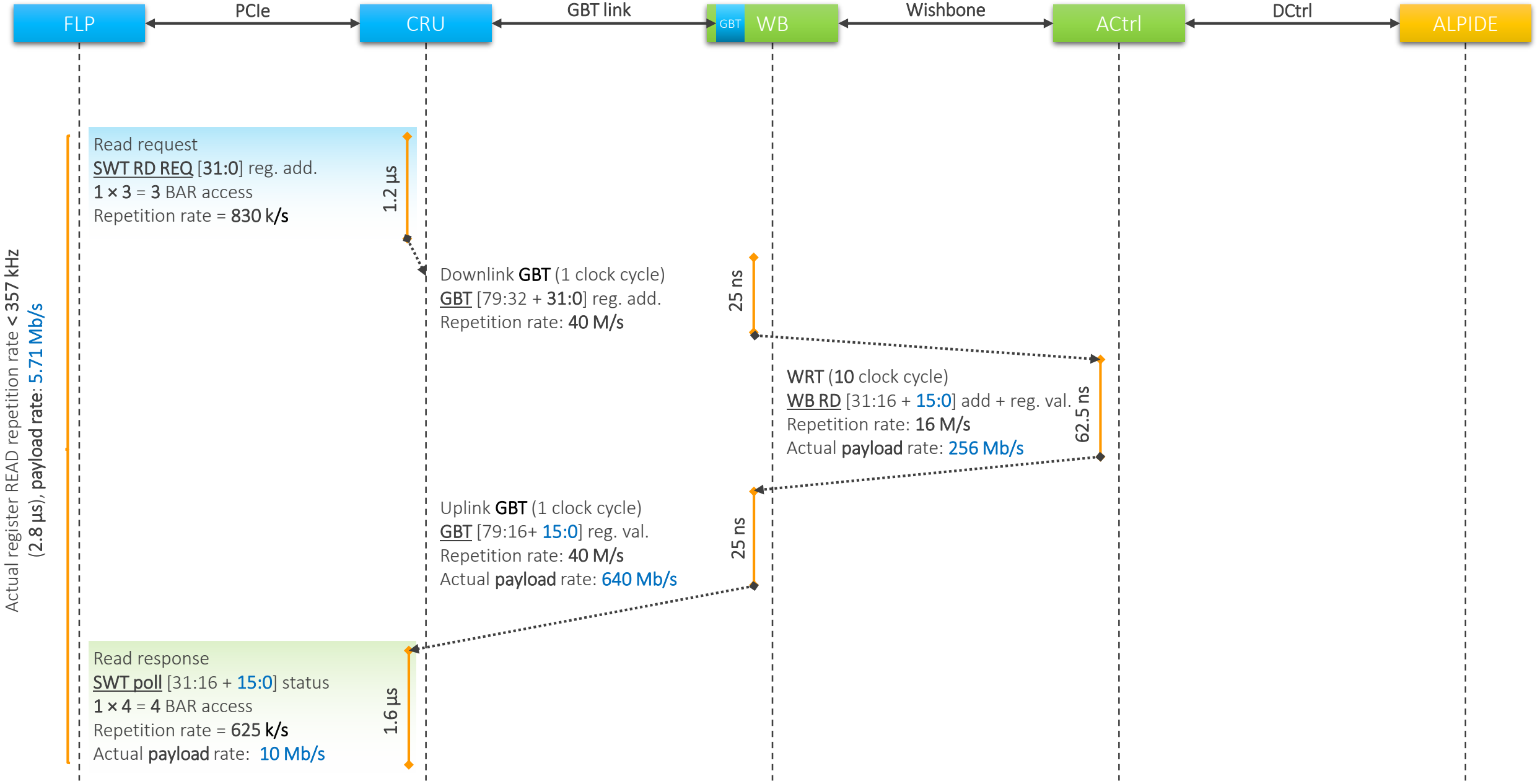
SWT Protocol CURRENT implementation – theoretical maximum payload and rates for different basic operations



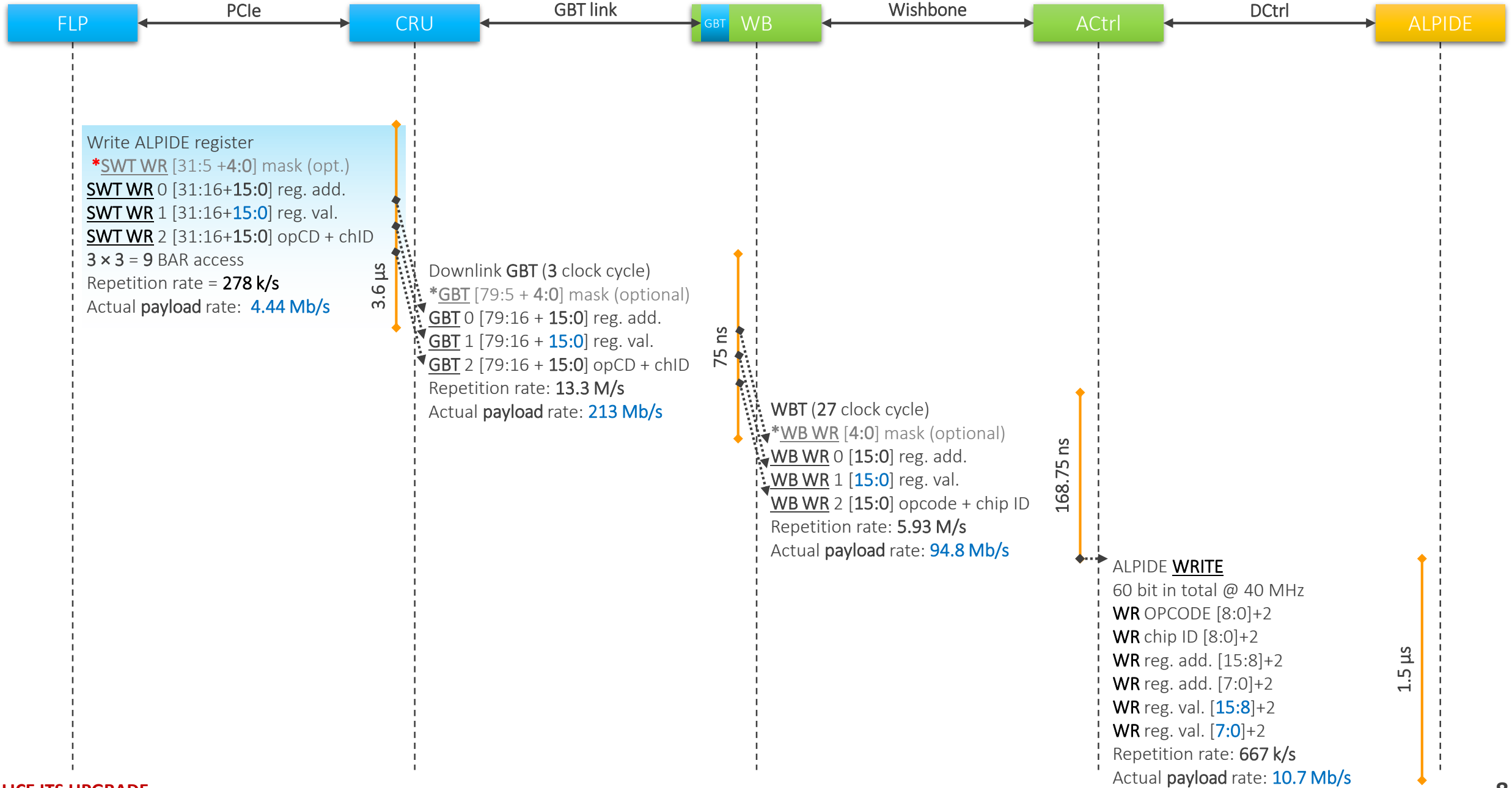
Writing to RU register with CURRENT implementation



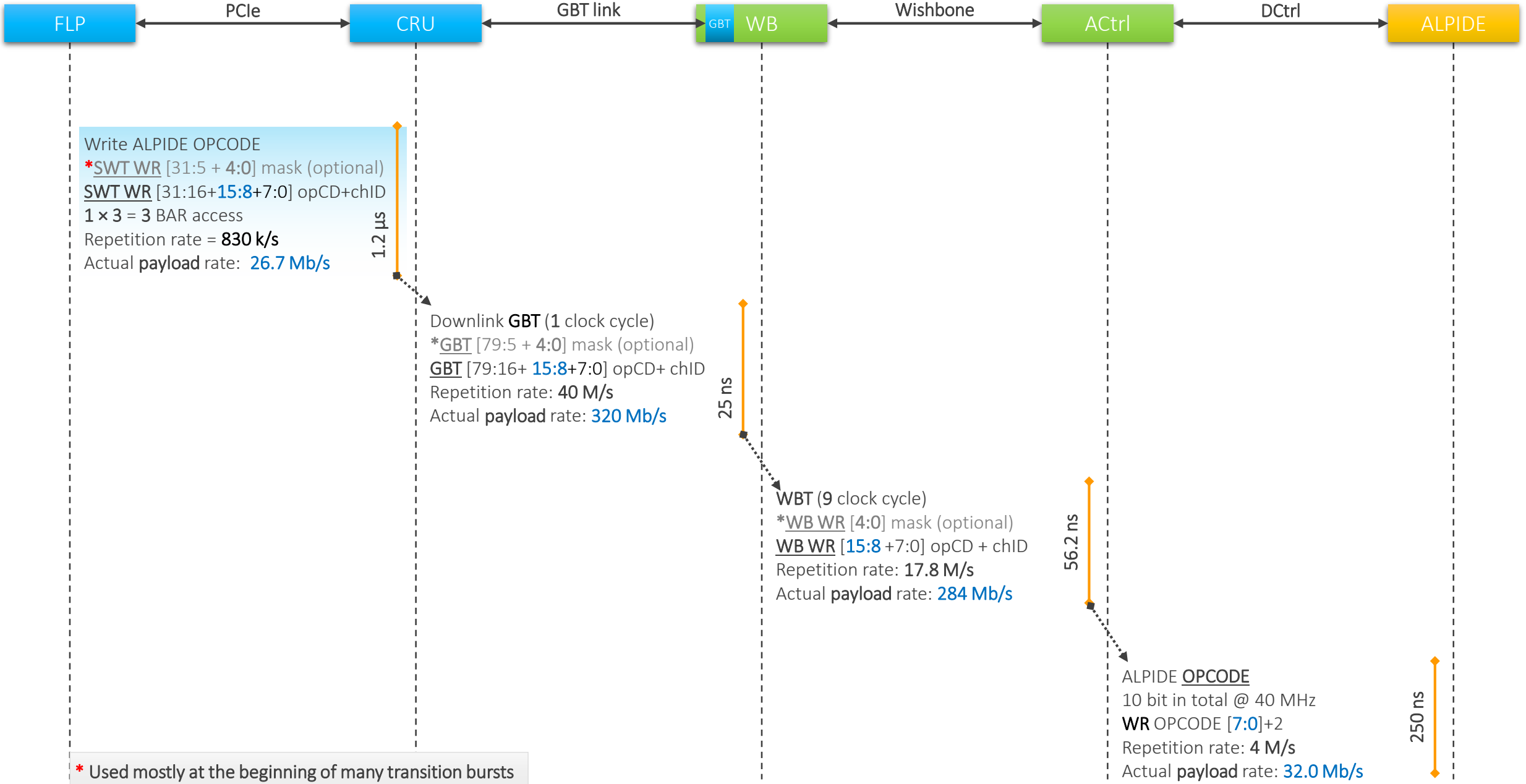
Reading from RU register with CURRENT implementation



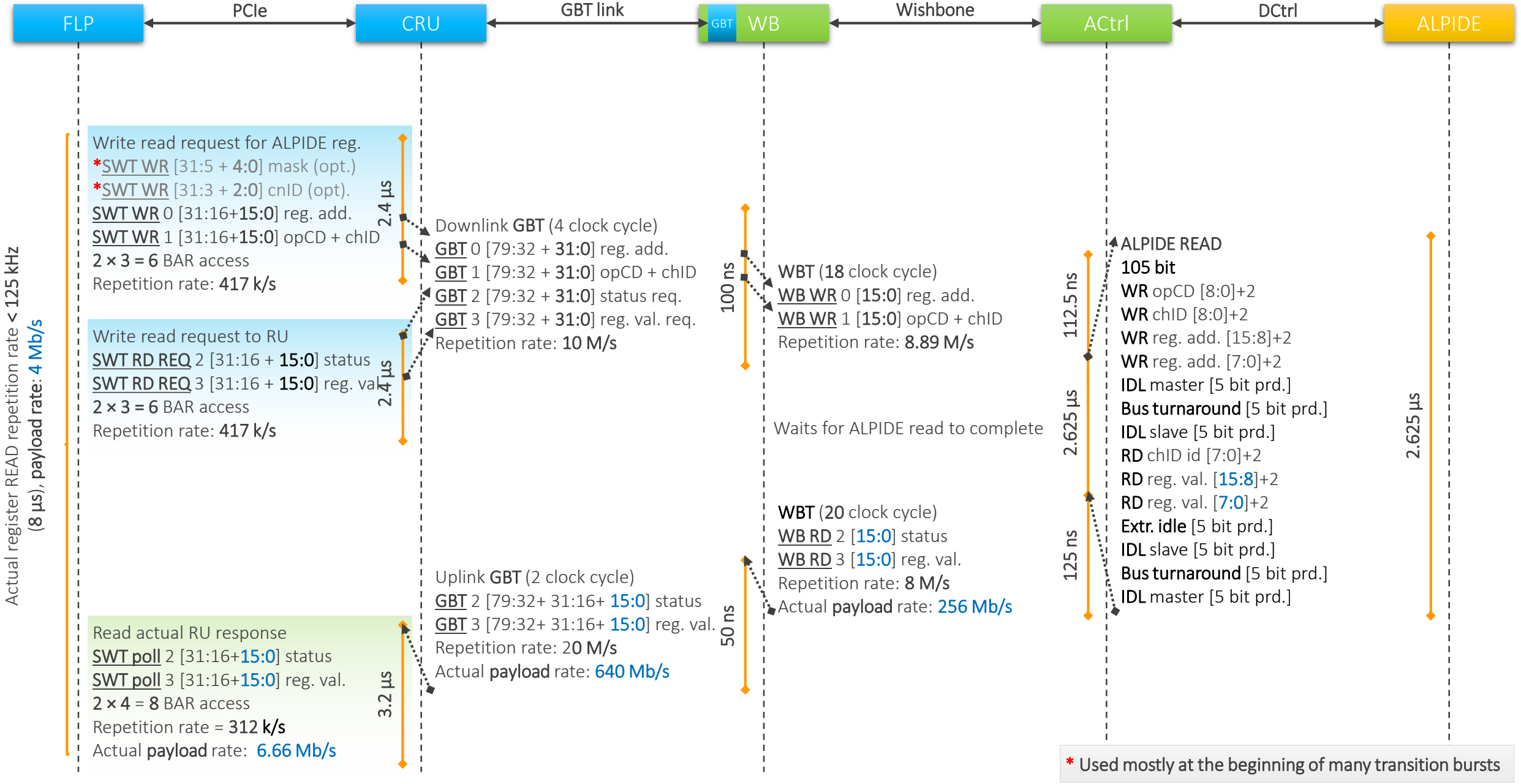
Actual **writing** to ALPIDE single register with **CURRENT** implementation

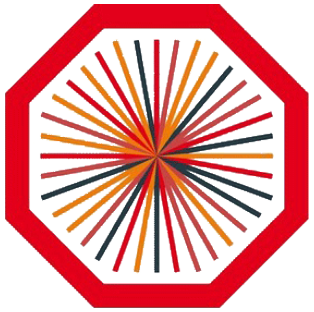


Actual **writing** to ALPIDE OPCODE (TRIGGER, PULSE, BCRST, etc.)



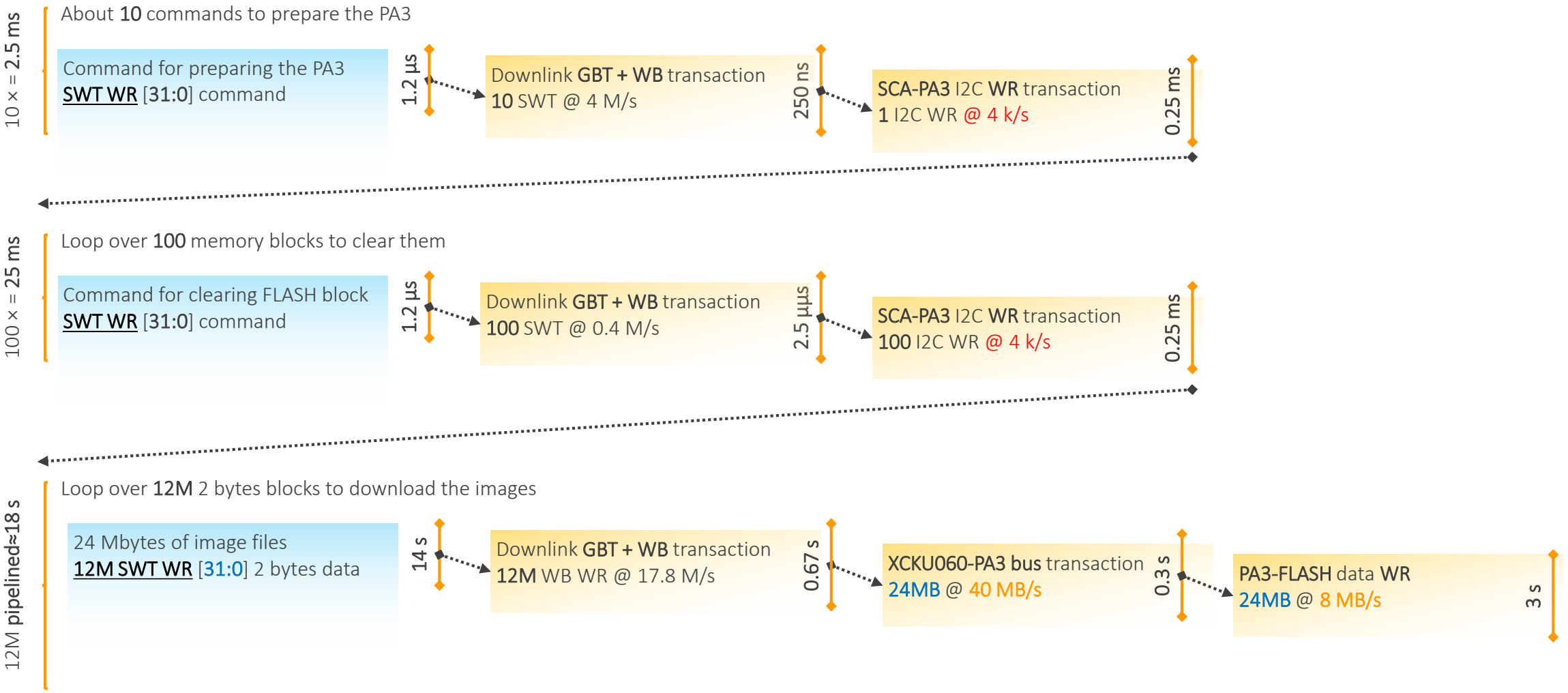
Actual **reading** from ALPIDE single register with **CURRENT** implementation

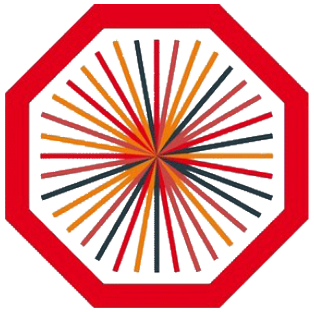




ITS readout slow control
FIRMWARE download

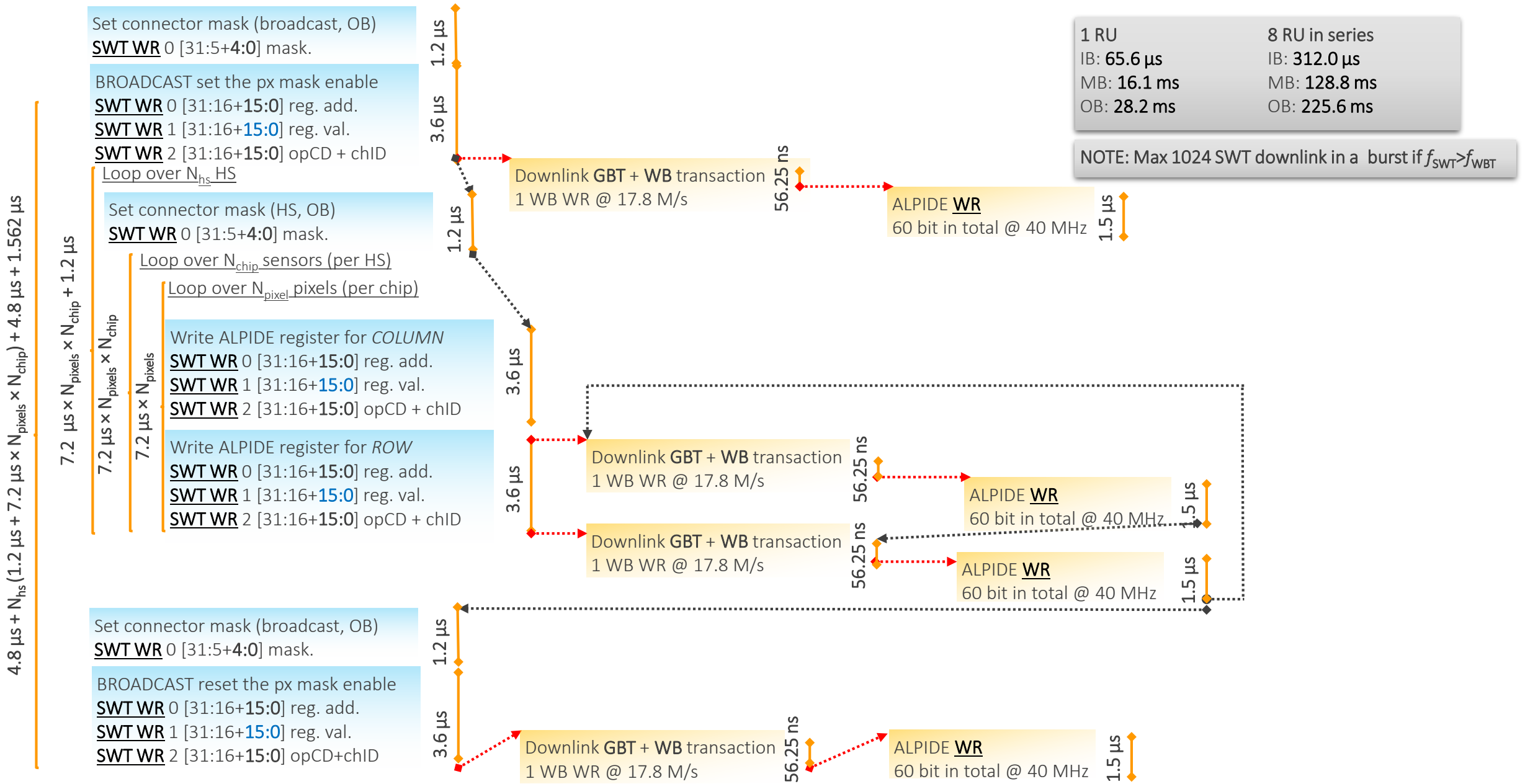
Firmware download through GBT-XCKU060-PA3 (fast, non rad-hard)



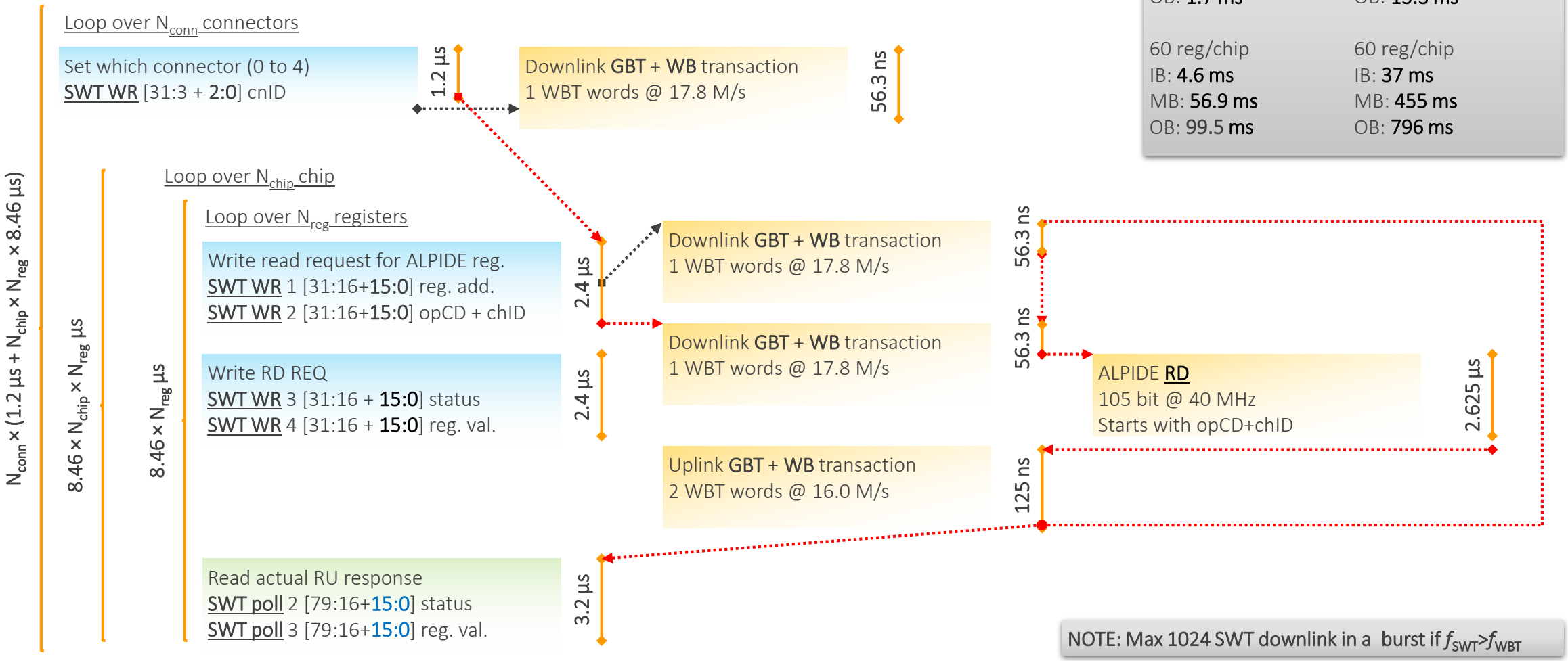


ITS readout slow control
ALPIDE operations

Masking pixels, without check (no read, 20 pixel per sensor)

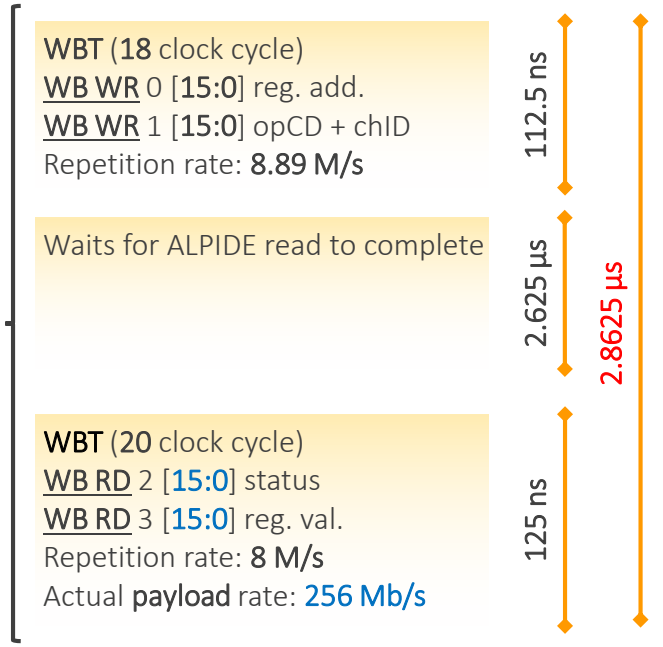


1 RU	8 RU in series
1 reg/chip	1 reg/chip
IB: **76.2 µs**	IB: **609.3 µs**
MB: **952.6 µs**	MB: **7.6 ms**
OB: **1.7 ms**	OB: **13.3 ms**
60 reg/chip	60 reg/chip
IB: **4.6 ms**	IB: **37 ms**
MB: **56.9 ms**	MB: **455 ms**
OB: **99.5 ms**	OB: **796 ms**

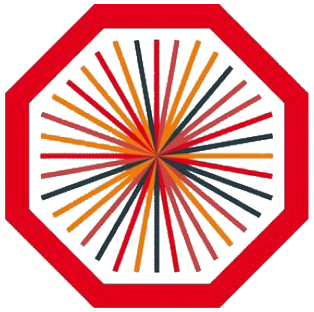


NOTE: Max 1024 SWT downlink in a burst if $f_{SWT} > f_{WBT}$

Abort gap summary (Simon's data)
- 1 abort gap: 119 × 25 ns = 2.975 µs
- LHC orbit: 11.2455 kHz, 2 abort gap per orbit
- Abort gap frequency: ≈ 22.5 kHz
- Abort gap availability: **66.91 ms/s** (6.7%)



Two registers per orbit (Simon's data)
- 22.5 kReg / s
- Payload (reg. value + status):
  32 bit × 22.5 kHz = 0.72 Mb/s



Backup / old

SWT Protocol CURRENT implementation – theoretical maximum payload rates

Single SWT write downlink (**5** BAR access)
WR SWT [75:64]
WR SWT [63:32]
WR SWT [31:0]
WR send request
WR reset request

Payload rate:
0.5 MSWT/s
16 Mb/s

Downlink (**1** clock cycle)
GBT word with 32 bit SWT payload
[79:76] SWT id
[75:32] unused
[31:0] WBT
Payload rate: 40 MSWT/s = 1.28 Gb/s

Downlink (**2** clock cycle)
WBT word with 16 bit payload
[31:16] WBT (address + w/r)
[15:0] WBT (data, payload)
Payload rate: 80 MWBT/s = 1.28 Gb/s

ALPIDE downlink (write to register)
WR opcode [8:0]+2
WR chip ID [8:0]+2
WR reg. add. [15:8]+2
WR reg. add. [7:0]+2
WR reg. val. [15:8]+2
WR reg. val. [7:0]+2

60 bit
Time: **1.5 µs**
Payload rate:
667 k/s
10.7 Mb/s

Single SWT read uplink (**11** BAR access)

Write read request **(1 SWT write**, 5 BAR**)**
WR SWT [75:64]
WR SWT [63:32]
WR SWT [31:0]
WR send request
WR reset request

Poll the data back (6 BAR access)
RD check status
WR read request
WR reset request
RD SWT [79:64]
RD SWT [63:32]
RD SWT [31:0]

Payload rate:
0.23 MSWT/s
7.3 Mb/s

Uplink (**1** clock cycle)
GBT word with 32 bit SWT payload
[79:76] SWT id
[75:32] unused
[31:0] WBT
Payload rate: 40 MSWT/s = 1.28 Gb/s

Uplink (**2** clock cycle)
WBT word with 16 bit payload
[31:16] WBT (address + w/r)
[15:0] WBT (data, payload)
Payload rate: 80 MSWT/s = 1.28 Gb/s

ALPIDE uplink (read from register)
WR opcode [8:0]+2
WR chip ID [8:0]+2
WR reg. add. [15:8]+2
WR reg. add. [7:0]+2
IDL master [5 bit prd.]
Bus trnd. [5 bit prd.]
IDL slave [5 bit prd.]
RD chip id [7:0]+2
RD reg. val. [15:8]+2
RD reg. val. [7:0]+2
Extr. idle [5 bit prd.]
IDL slave [5 bit prd.]
Bus trnd. [5 bit prd.]
IDL master [5 bit prd.]

105 bit
Time: **2.625 µs**
Payload rate:
378 k/s
6.0 Mb/s

SWT Protocol SMART implementation – theoretical maximum payload rates

Single SWT write downlink (**3** BAR access)
WR SWT [31:0]
WR send request
WR reset request
Max rate:
0.83 MSWT/s
26.7 Mb/s

Downlink (**1** clock cycle)
GBT word with 32 bit SWT payload
[79:32] unused & [31:0] SWT
Max rate: 40 MSWT/s = 1.28 Gb/s

Downlink (**2** clock cycle)
WBT word with 16 bit payload
[15:0] WBT
Payload rate: 80 MWBT/s = 1.28 Gb/s

ALPIDE downlink (write to register)
60 bit transaction, **1.5 µs**
Max rate: 667 kreg/s = 10.7 Mb/s

Single SWT read uplink (**6** BAR access)
WR SWT [31:0]
WR send request
WR reset request
WR
RD check status
RD SWT [31:0]
Max rate:
0.42 MSWT/s
13.3 Mb/s

Uplink (**1** clock cycle)
GBT word with 32 bit SWT payload
[79:32] unused & [31:0] SWT
Max rate: 40 MSWT/s = 1.28 Gb/s

Uplink(**2** clock cycle)
WBT word with 16 bit payload
[15:0] WBT
Max rate: 80 MWBT/s = 1.28 Gb/s

ALPIDE uplink (read from register)
105 bit transaction, **2.625 µs**
Max rate: 378 k/s = 6.0 Mb/s

SWT Protocol OPTIMAL implementation (**requires modification the CRU FPGA design**) – theoretical maximum payload rates

Single SWT write downlink (1 BAR access)
WR SWT [31:0]
Max rate:
2.5 MSWT/s
80 Mb/s

Downlink (**1** clock cycle)
GBT word with 32 bit SWT payload
[79:32] unused & [31:0] SWT
Max rate: 40 MSWT/s = 1.28 Gb/s

Downlink (**2** clock cycle)
WBT word with 16 bit payload
[15:0] WBT
Payload rate: 80 MWBT/s = 1.28 Gb/s

ALPIDE downlink (write to register)
60 bit transaction, **1.5 µs**
Max rate: 667 kreg/s = 10.7 Mb/s

Single SWT read uplink (2 BAR access)
RD check status
RD SWT [31:0]
Max rate:
1.25 MSWT/s
40 Mb/s

Uplink (**1** clock cycle)
GBT word with 32 bit SWT payload
[79:32] unused & [31:0] SWT
Max rate: 40 MSWT/s = 1.28 Gb/s

Uplink(**2** clock cycle)
WBT word with 16 bit payload
[15:0] WBT
Max rate: 80 MWBT/s = 1.28 Gb/s

ALPIDE uplink (read from register)
105 bit transaction, **2.625 µs**
Max rate: 378 k/s = 6.0 Mb/s