FELIX/GTM Interface

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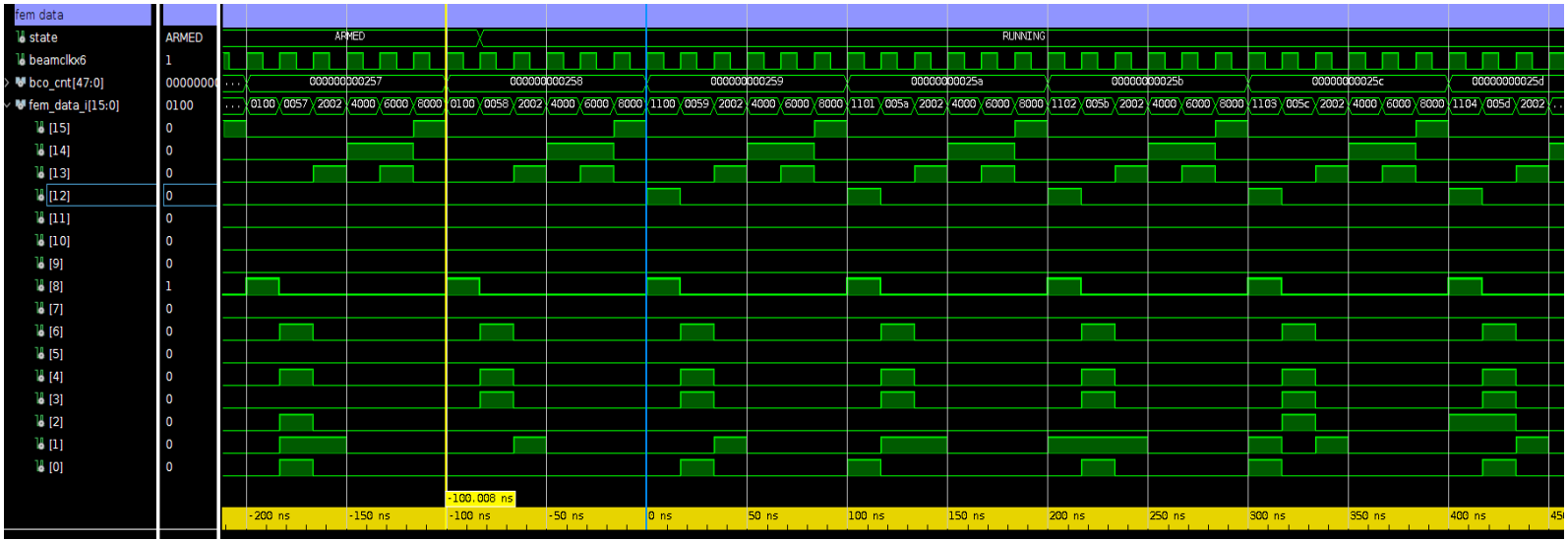
MVTX RU & Firmware Meeting

GTM Bit Distribution

clock count		0	1	2	3	4	5
bits 0-7	mode bits/BCO	mode bits	BCO bits 0-7	BCO bits 8-15	BCO bits 16-23	BCO bits 24-31	BCO bits 32-39
bit 8	beam clock	1	0	0	0	0	0
bit 9	LVL1 accept	X	0	0	0	0	0
bit 10	endat0	X	X	X	X	X	X
bit 11	endat1	X	X	X	X	X	X
bit 12	modebit en.	1	0	0	0	0	0
bits 13-15		3 user bits	0	1	2	3	4



FELIX GTM Receiver

The VHDL code in gtm_recvr.vhd sets the bits from the GTM RX as:

```
if (rx_kcode(1) = '0'
and rx_disparty_error = x"0"
and rx_invalid_char = x"0") then
    mode_bits_en <= rx_data(10);
    level_1_accept <= rx_data(9);
    end_dat <= rx_data(12 downto 11);
    user_bits <= rx_data(15 downto 13);
    beam_clk <= rx_data(8);
else
    (Set everything to 0)
```

	Bits from GTM	Bits set in FELIX
Mode bits / BCO	0-7	0-7
Beam Clock	8	8
LVL1 Accept	9	9
End Data	10-11	11-12
Mode Bit Enable	12	10
User Bits	13-15	13-15

I checked the bit pattern in the GTM document from May 2020 as well

FPGA Pins

```
#MVTX GTM
#refclk from LMK OUT2
#set_property PACKAGE_PIN Y37  [get_ports GTM_GTREFCLK_P_IN]
#set_property PACKAGE_PIN Y38  [get_ports GTM_GTREFCLK_N_IN]
#refclk from LMK OUT6
 set_property PACKAGE_PIN P8   [get_ports GTM_GTREFCLK_P_IN]
 set_property PACKAGE_PIN P7   [get_ports GTM_GTREFCLK_N_IN]
#set_property PACKAGE_PIN AA43 [get_ports GTM_RX_P]
#set_property PACKAGE_PIN AA44 [get_ports GTM_RX_N]
#set_property PACKAGE_PIN Y41  [get_ports GTM_TX_P]
#set_property PACKAGE_PIN Y42  [get_ports GTM_TX_N]
#MVTX GTM end
```