Testing MVTX Readout Units

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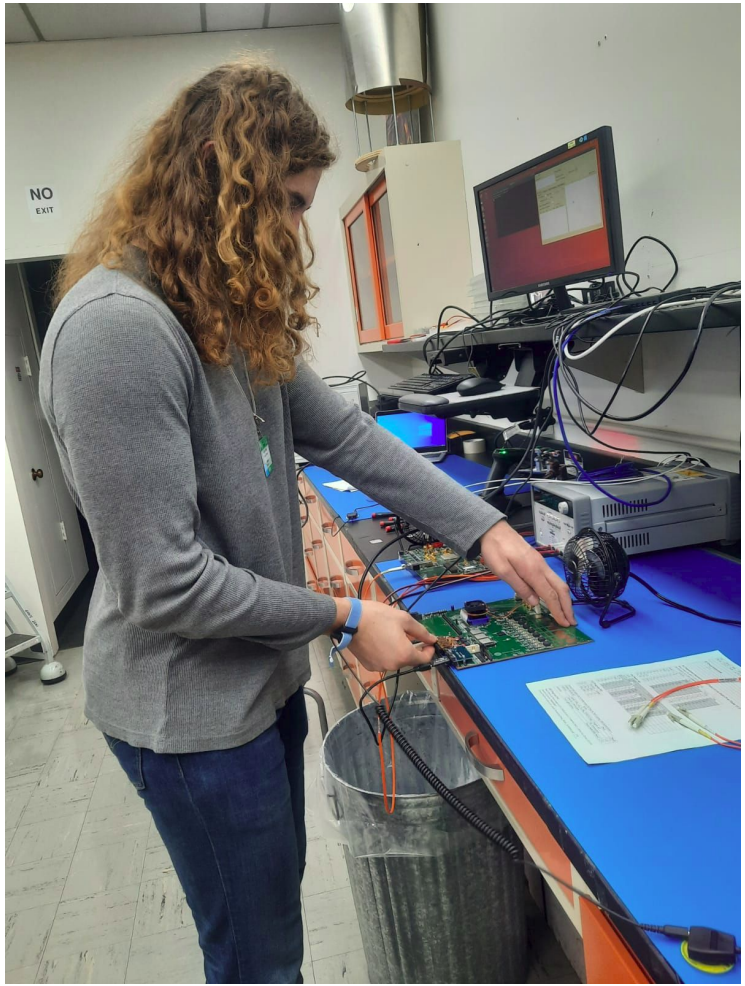
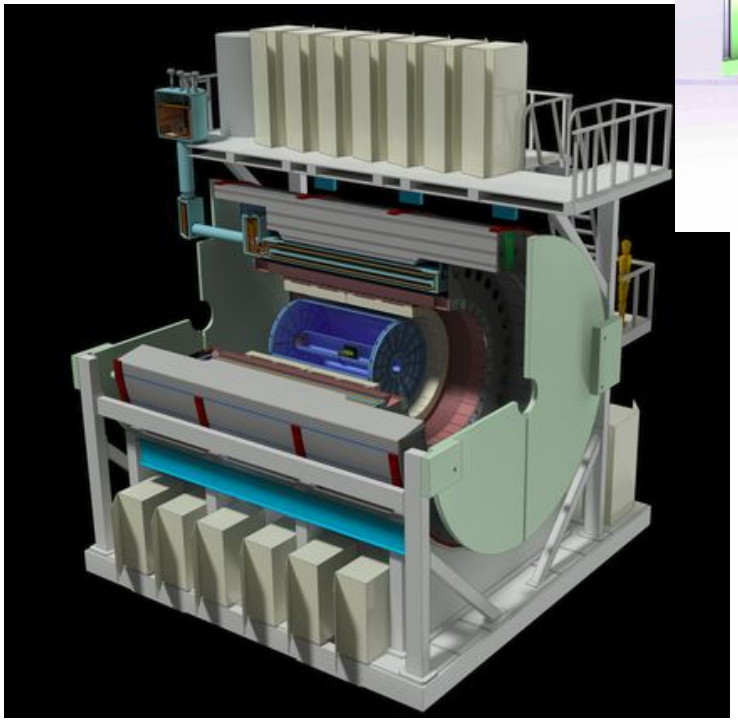
For the sPHENIX Collaboration

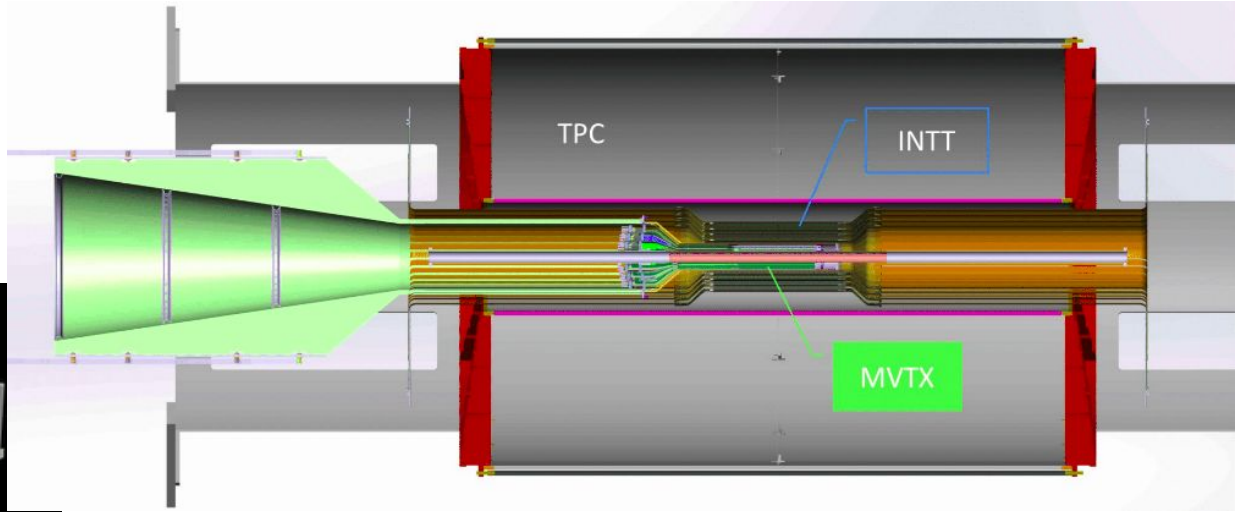
Outline

- The sPHENIX detector
- MVTX readout system
- MVTX readout unit
- Testing and results
- Assembly
- Conclusion



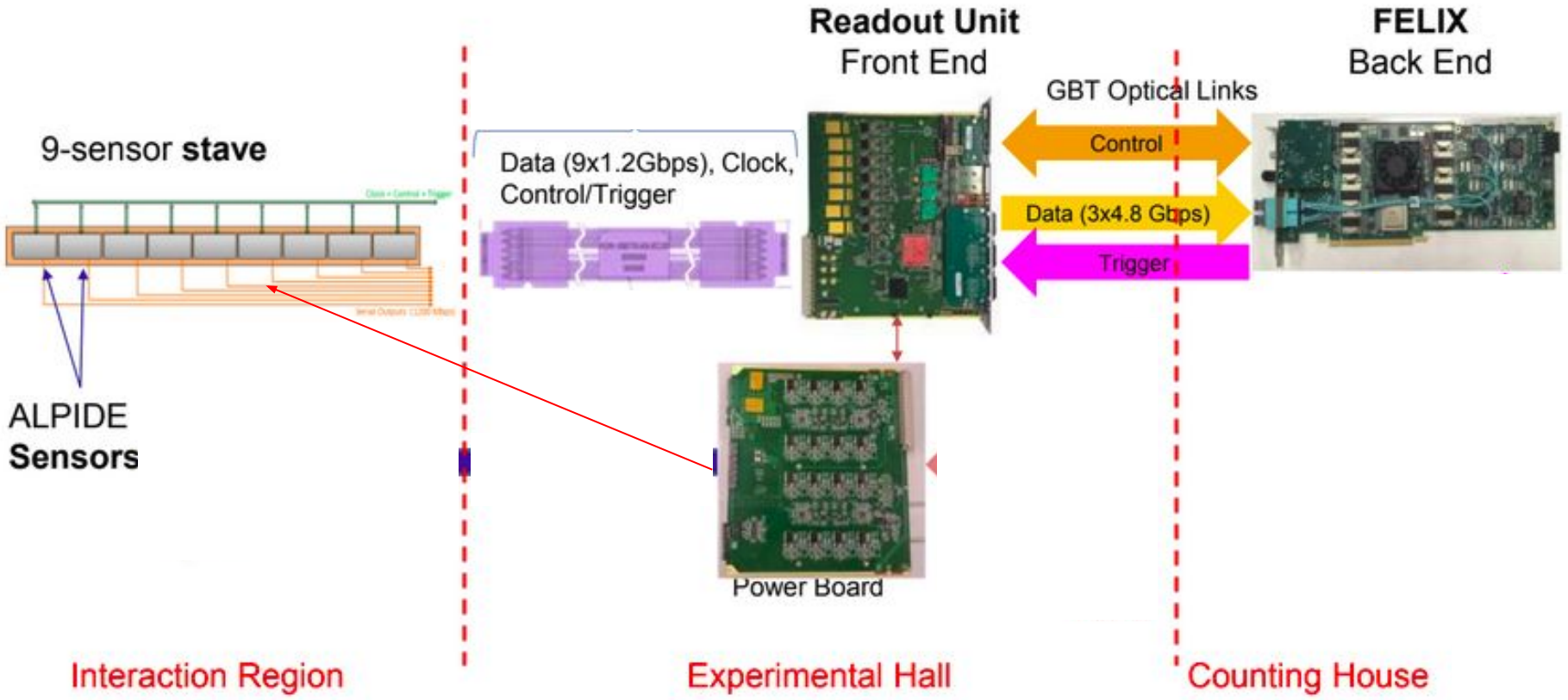
sPHENIX Detector

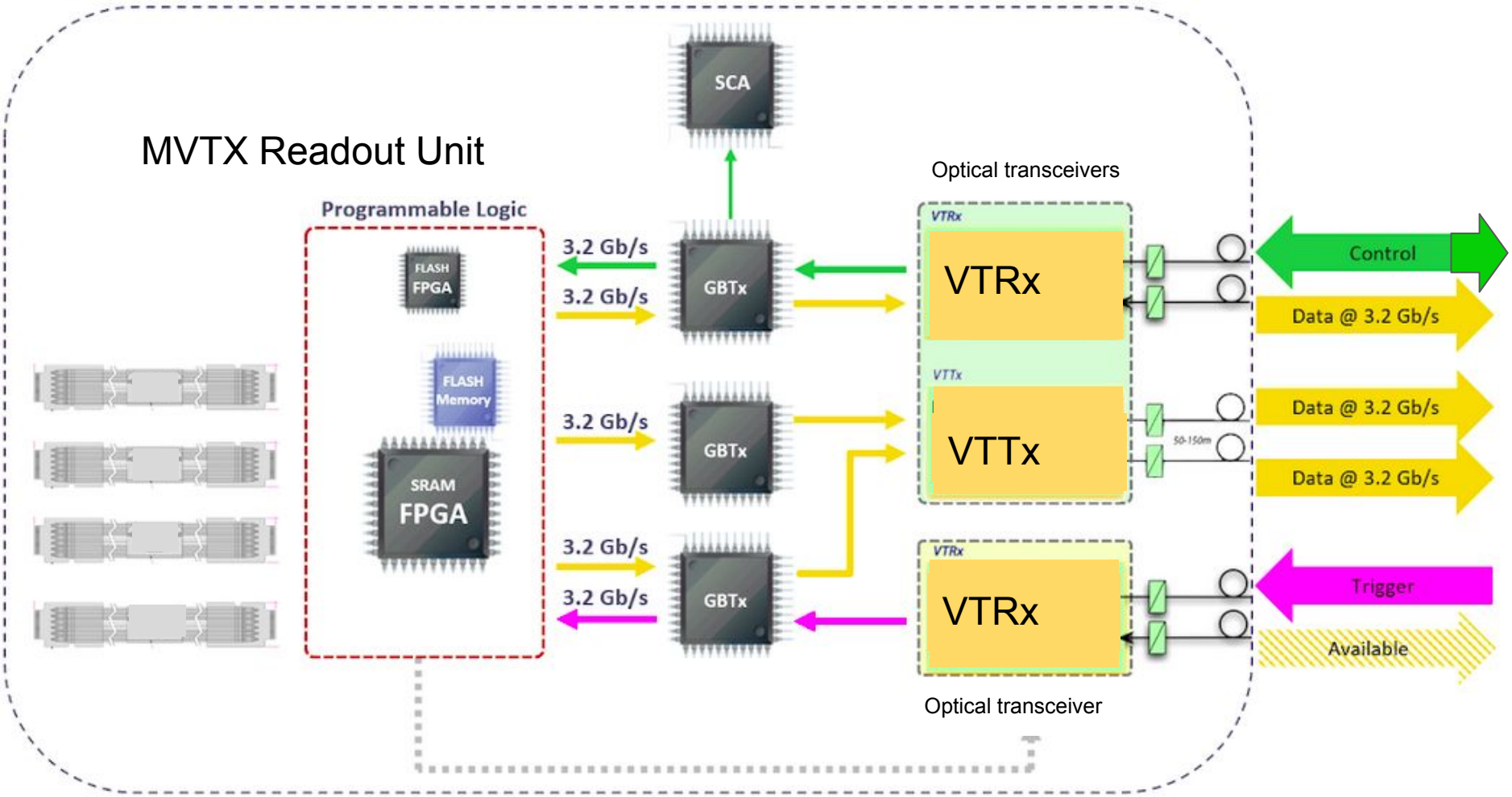




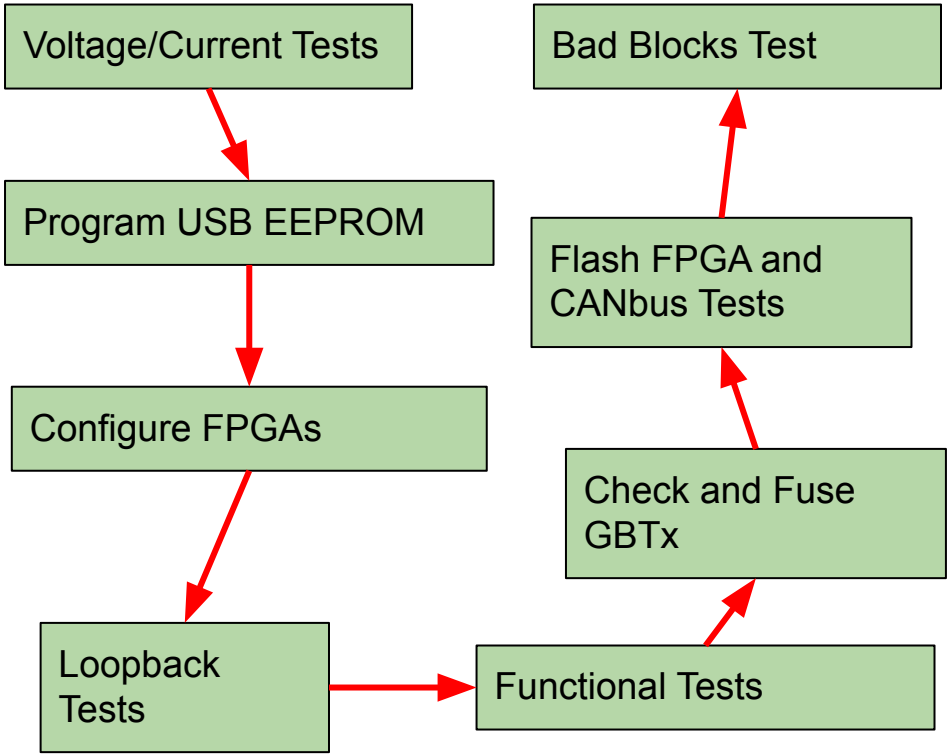
- MAPS-based VerTeX detector (MVTX)
  - Tracking and vertexing
  - Heavy-flavor studies
  - Fine pitch
  - Fast, high efficiency, low noise
  - Ultra thin
  - On-pixel digitization

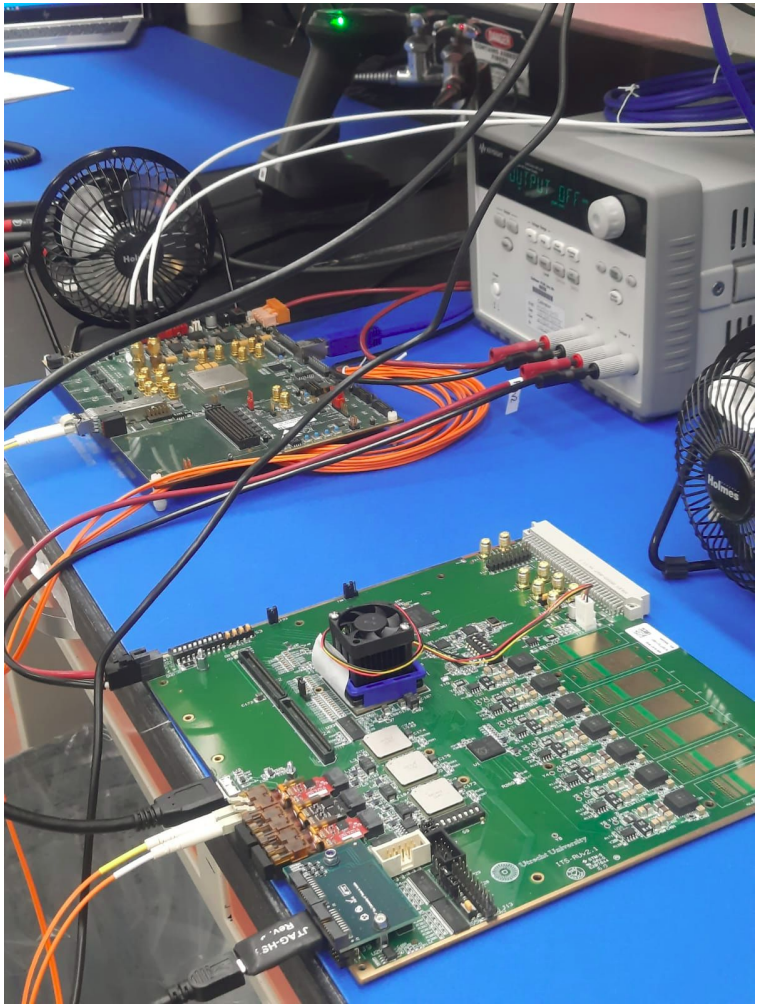
MVTX Readout System




MVTX Readout Unit
SCA
Programmable Logic
FLASH FPGA
FLASH Memory
SRAM FPGA
3.2 Gb/s
3.2 Gb/s
GBTx
3.2 Gb/s
3.2 Gb/s
GBTx
3.2 Gb/s
3.2 Gb/s
GBTx
Optical transceivers
VTRx
VTRx
VTTx
VTTx
VTRx
VTRx
Optical transceiver
Control
Data @ 3.2 Gb/s
Data @ 3.2 Gb/s
Data @ 3.2 Gb/s
Trigger
Available

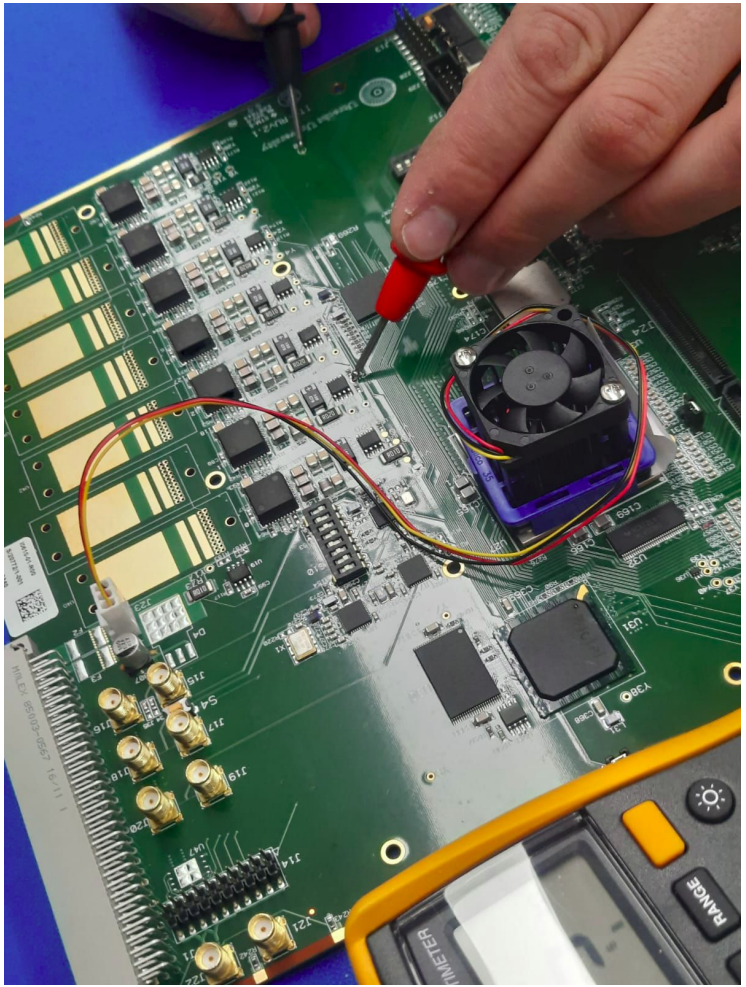
Readout Unit Testing Steps





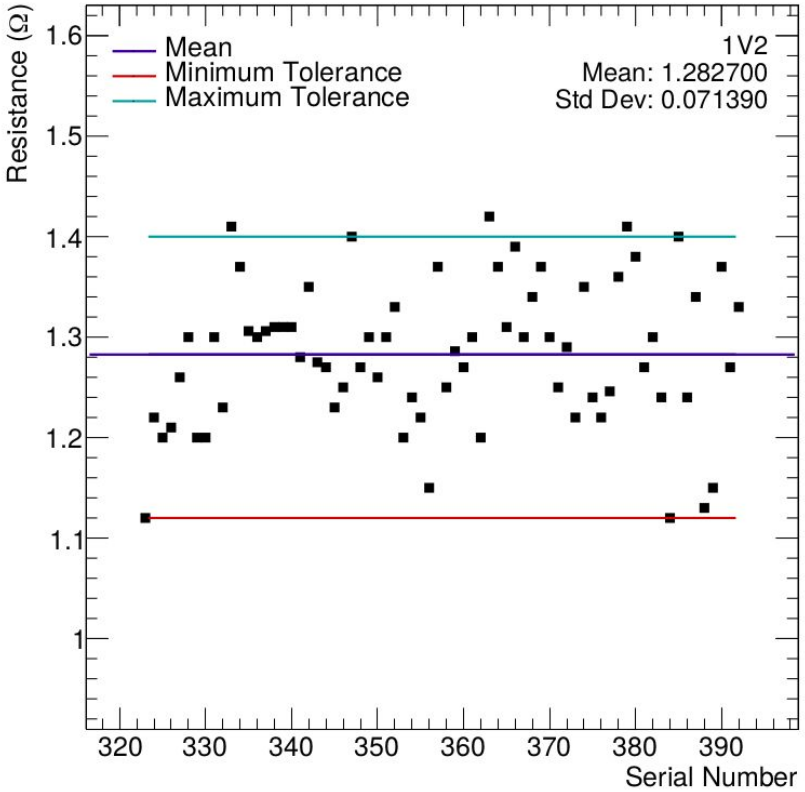
Voltage/Current Tests & Program USB EEPROM

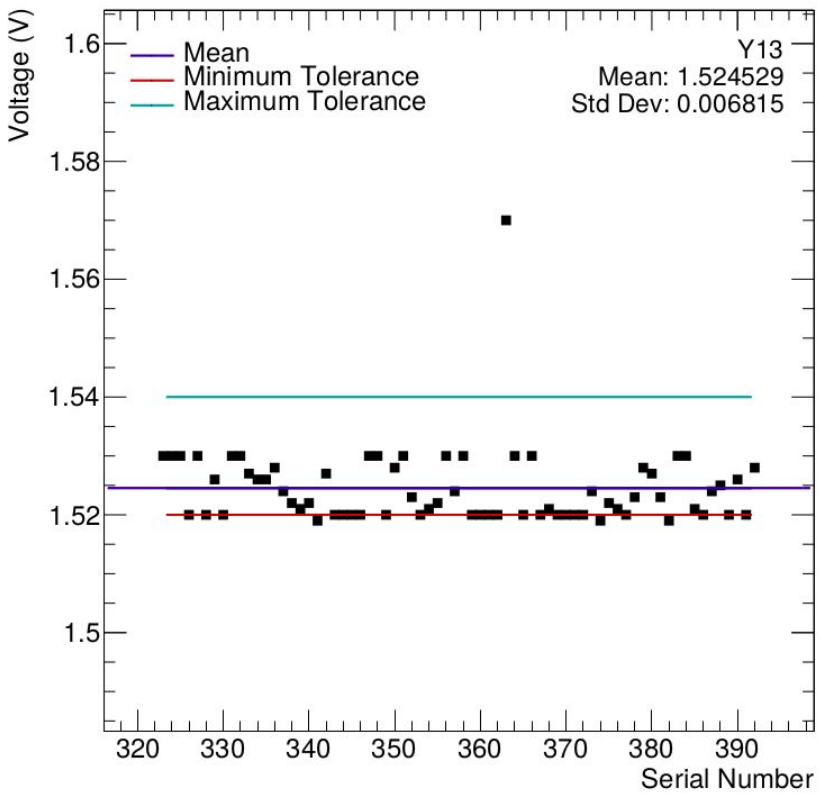
- Test for short circuits
- Power on and voltage tests
- Program USB EEPROM



Voltage/Current Tests

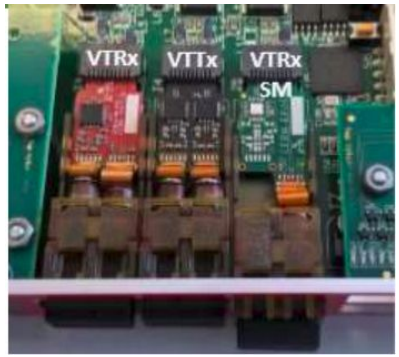
- Out-of-range values did not impact functionality

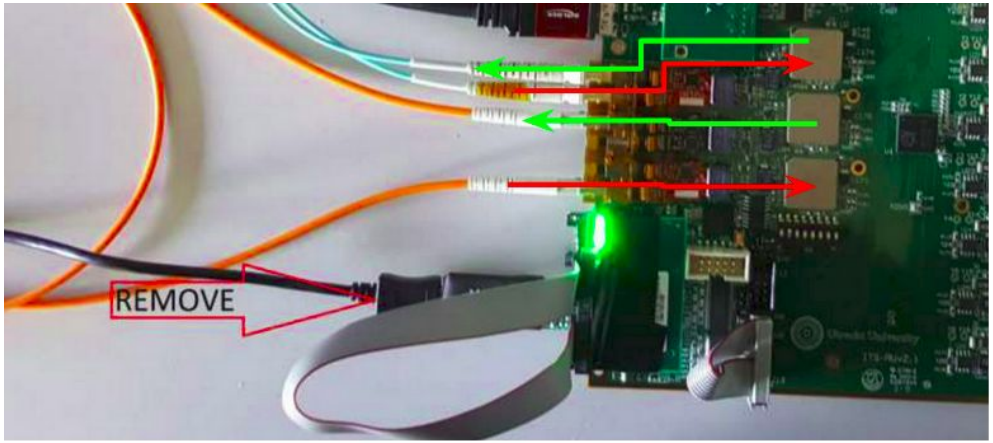


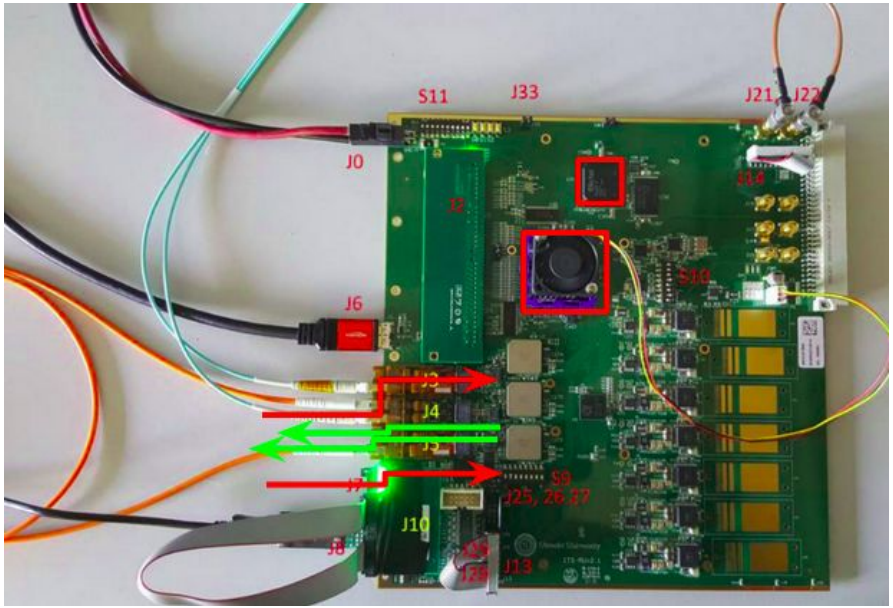


Configure FPGAs, Loopback & Functional Tests

- Program flash FPGA
- Configure main FPGA
- Long and short loopback test
- Check SCA ADC values
- Functional checks

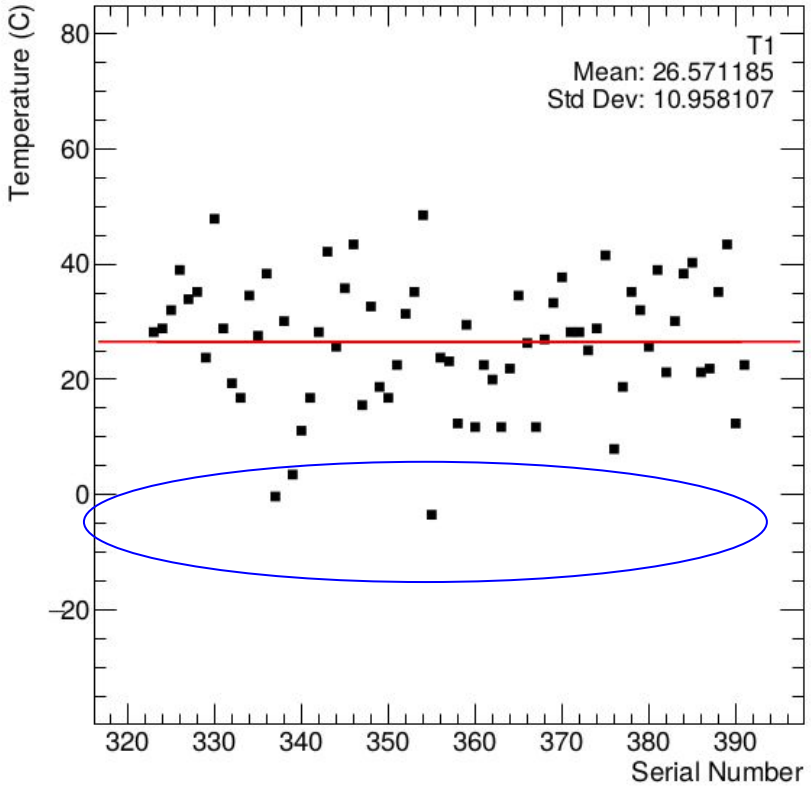


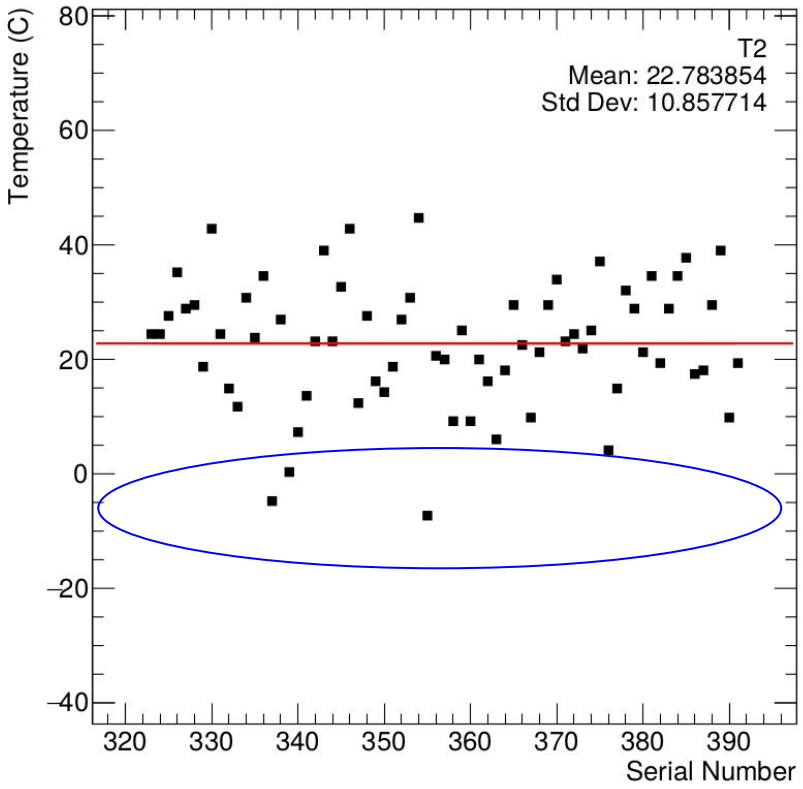




Slow Controls ADC Values

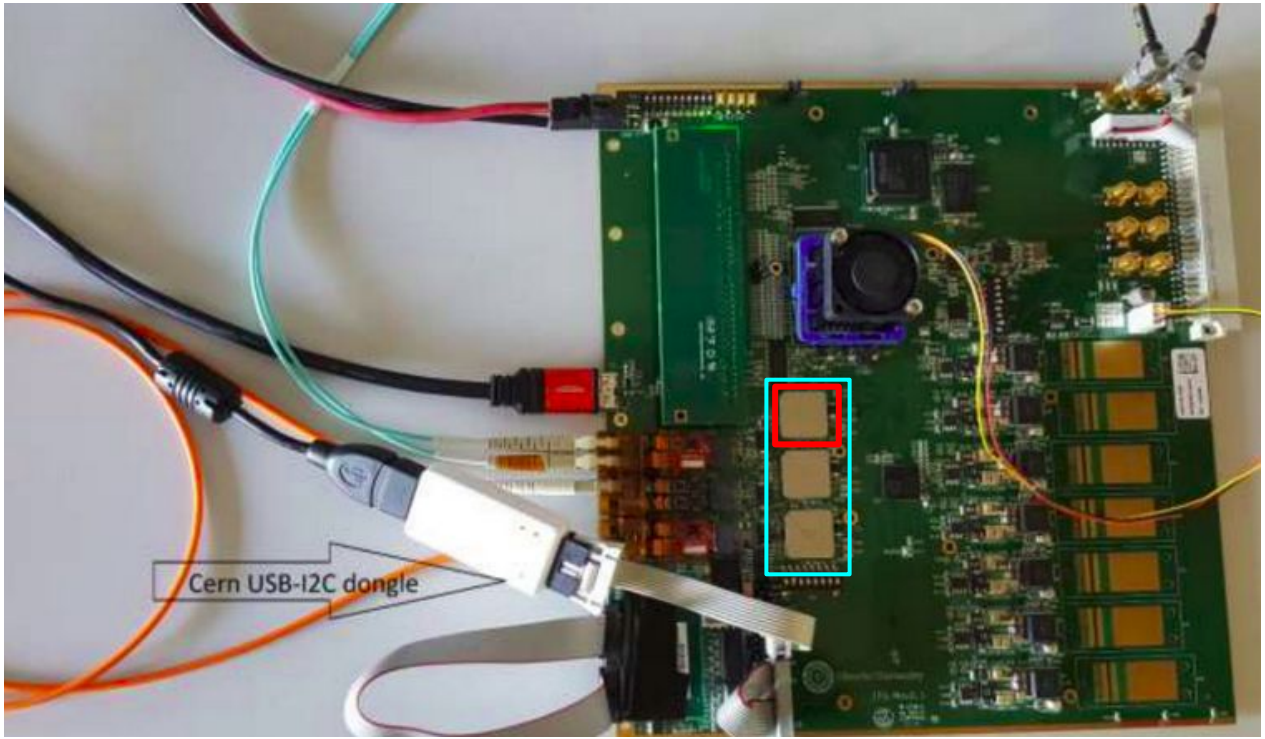
- Need to recalibrate several temperature sensors





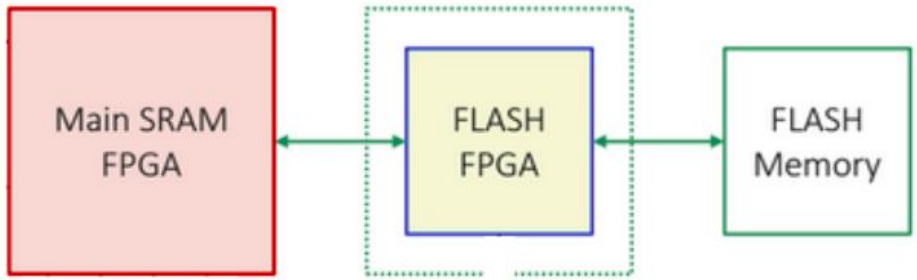
Check & Fuse GBTx0

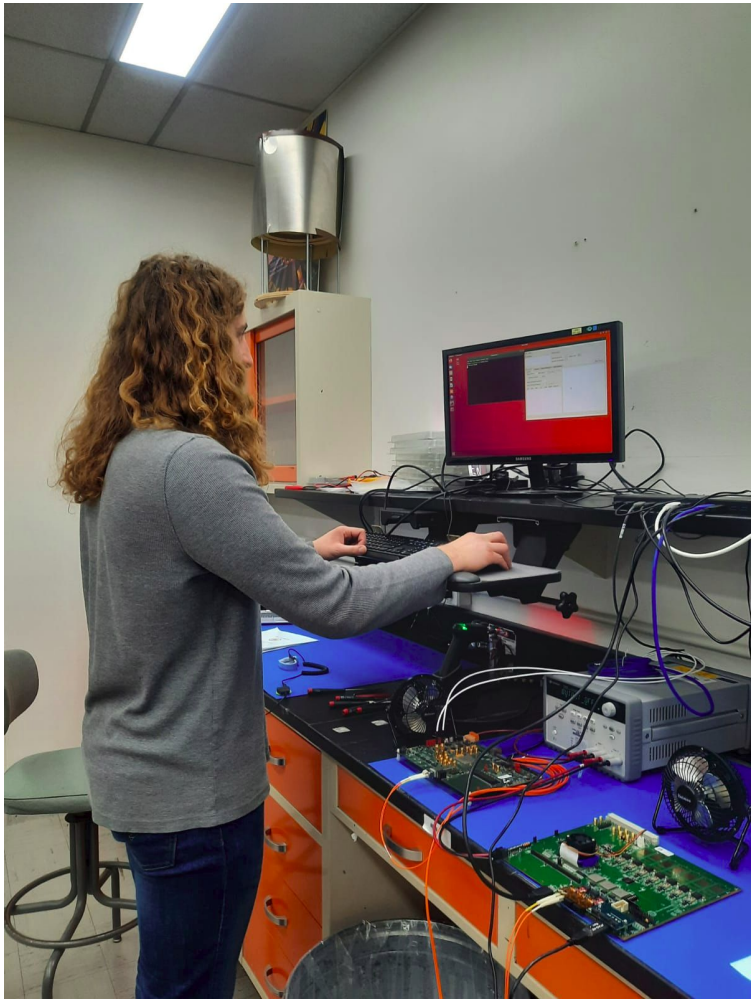
- Detect presence of all three GBTx
- Fuse GBTx0



Flash FPGA and CANbus Tests

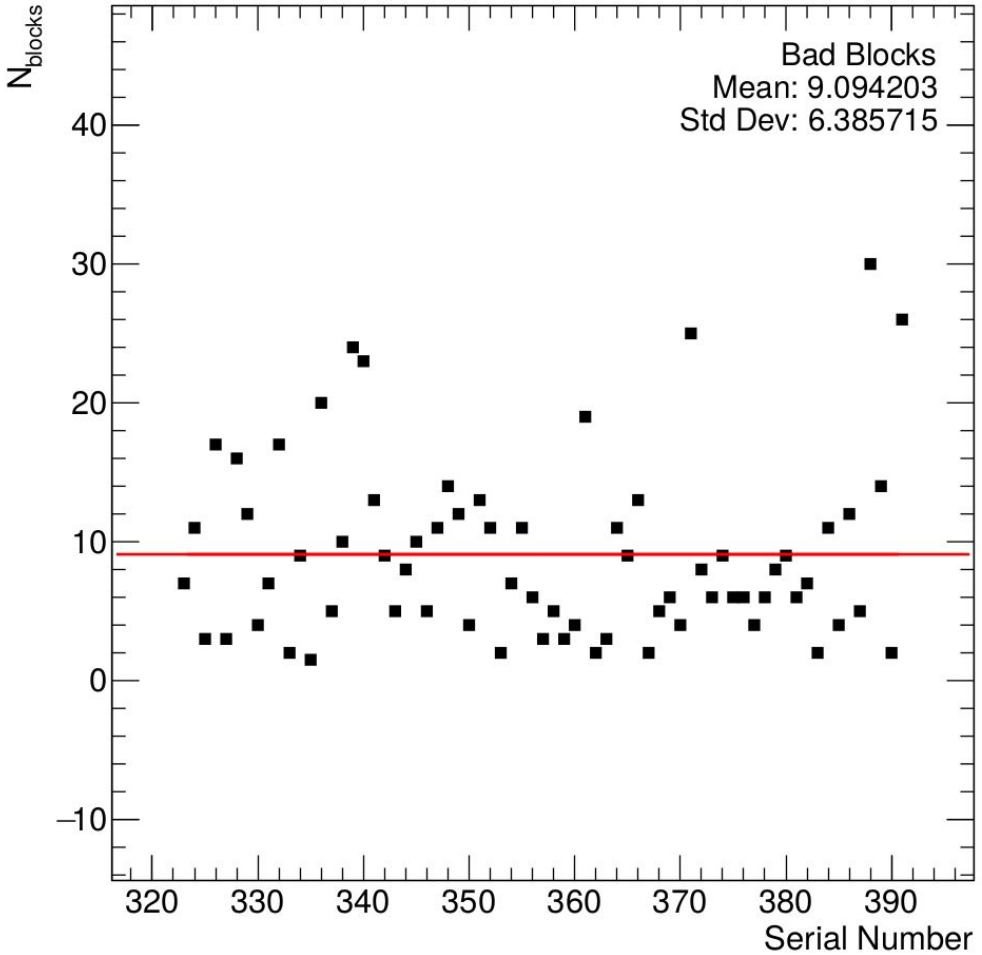
- Program flash FPGA for detector use
- SCA links
- Main FPGA select map interface
- Flash interface
- Test CANbus





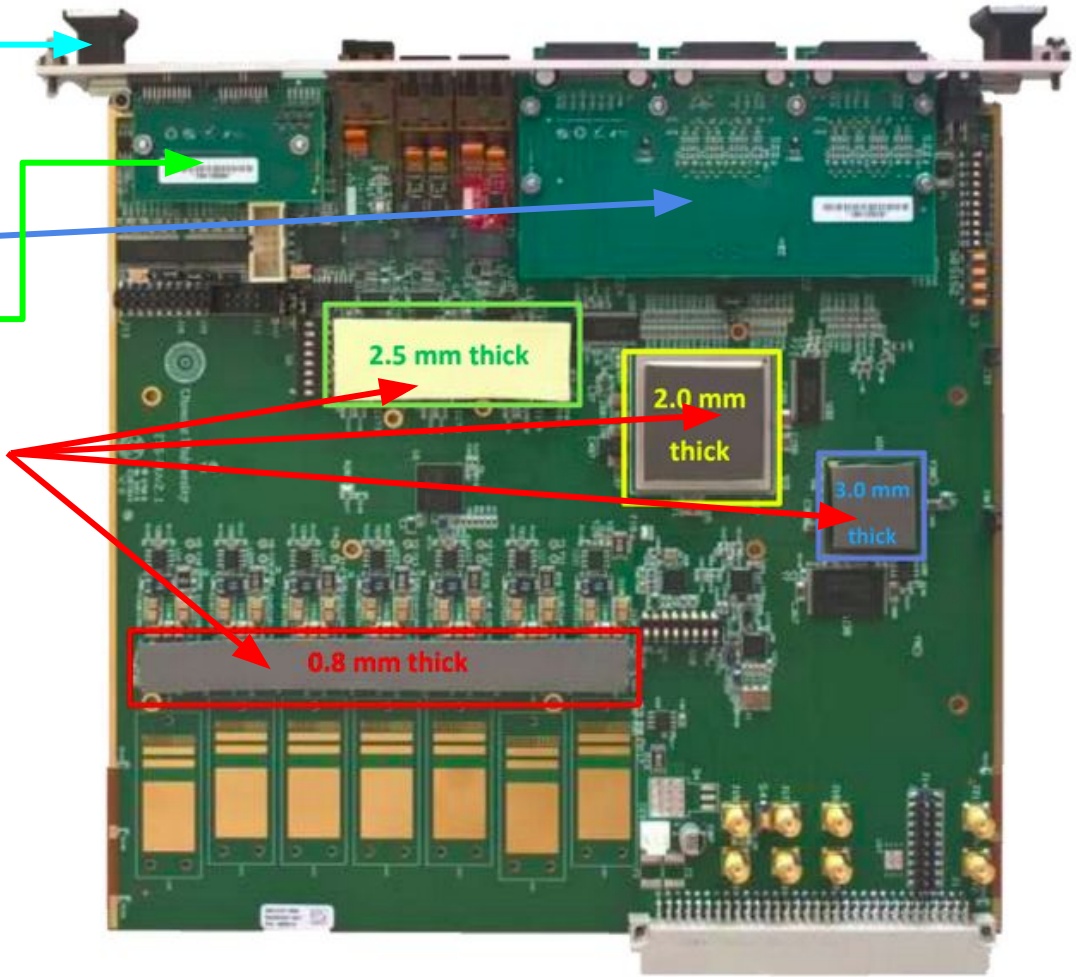
Bad Blocks Test

- Flash memory mapped
- All within acceptable range



Assembly

- Transition board
- Power mezzanine
- Front panel
- Thermal pads & cold plate



Conclusions

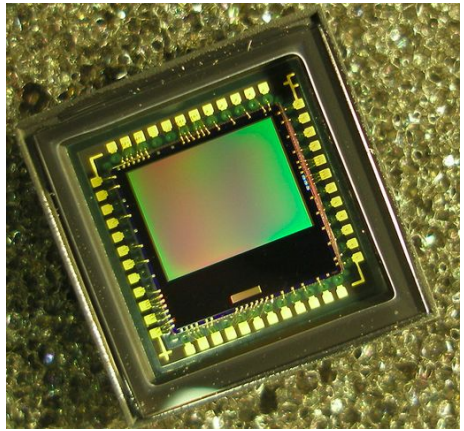
- Testing at ORNL is going well and on schedule
- Only one board left to debug
- Next steps

  - Test with stave and ATLAS FELIX back-end

  - Ship readout units to Brookhaven for further testing

RUv2 Testing and Assembly Team at ORNL:

- Jo Schambach
- Friederike Bock



Backup

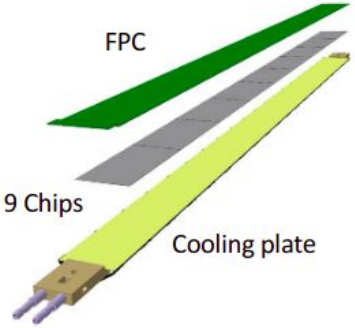
“sPHENIX will provide state-of-art capabilities for studies of the strongly interacting quark-gluon plasma using jet and heavy-flavor observables.”

- https://www.sphenix.bnl.gov/

Monolithic-Active-Pixel-Sensors (MAPS)

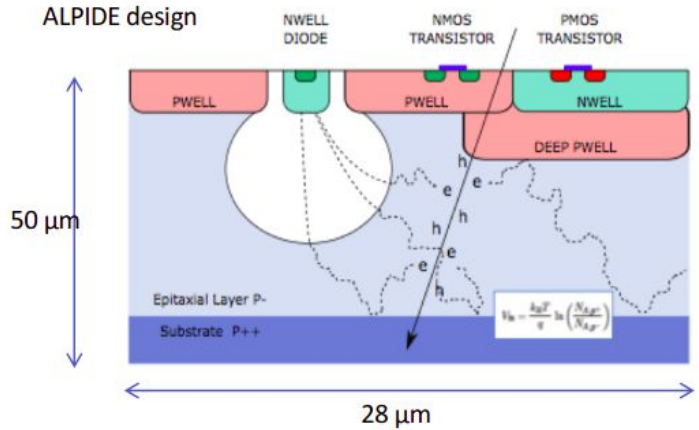
The next Generation State of the Art Pixel Tracker

- Advantages of ALICE MAPS/ALPIDE:
  - Very fine pitch (27x29 µm)
  - High efficiency (>99%) and low noise ($<10^{-6}$)
  - Fast readout, ~5 µS
  - Ultra-thin/low mass, 50µm (~0.3% X_0)
  - On-pixel digitization, low power dissipation



A 9-chip MAPS stave, 1.5 x 27cm²

An ideal detector for QGP b-jet physics!



Tower Jazz 0.18 µm CMOS

- feature size 180 nm
- metal layers 6
- gate oxide 3nm

substrate: $N_A \sim 10^{18}$
epitaxial layer: $N_A \sim 10^{13}$
deep p-well: $N_A \sim 10^{16}$

MVTX Readout System