Testing sPHENIX MVTX Readout Units

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sPHENIX Experiment

- Study the structure and behavior of the quark-gluon plasma
- State-of-art capabilities for precision measurements of jet and heavy-flavor observables

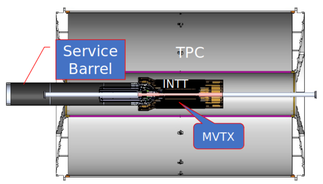

Figure 1: Cutaway view of the sPHENIX detector, highlighting the IINT, MVTX, and TPC.

Maps-Based Vertex Detector (MVTX)

- Used for tracking and vertexing
- Located in the central barrel around the interaction point
- 2π acceptance in azimuth and $|\eta| < 1$ in pseudorapidity

Data Flow

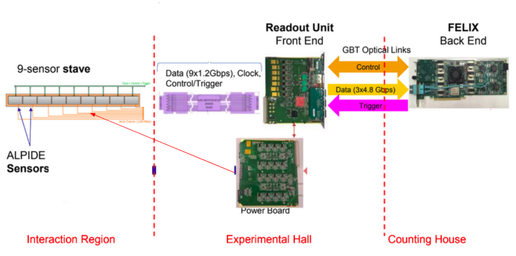

Figure 2: Representation of the flow of data through the detector system.

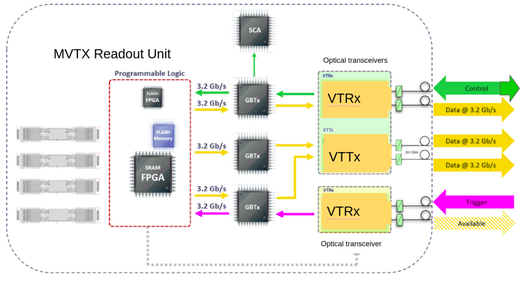

Figure 3: Representation of the flow of data through the front end readout boards

Test for Short Circuits & Program USB EEPROM

- Impedance testing for short circuits[Fig. 4]
- Power on and test rail voltages/currents
- Most measured values were consistent with expectations[Fig. 5]
- Outliers caused no impact to functionality →Used for spares
- Program USB EEPROM, allowing communication with main FPGA

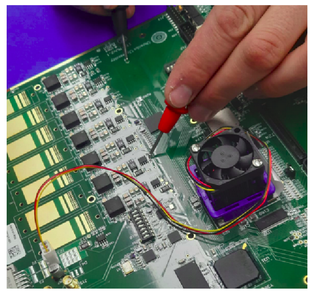

Figure 4: Impedance testing at ORNL

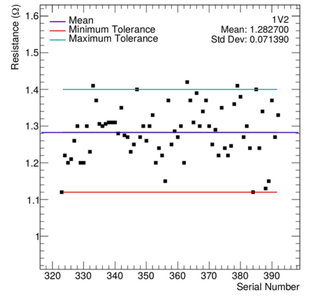

Figure 5: Example impedance testing plot.

Configure FPGAs, loopback, and functional tests

- Experiment →Programming loaded into flash memory
- Testing →Programming loaded into flash FPGA
- Long[Fig. 6] and short[Fig. 7] loopback tests performed to test data paths

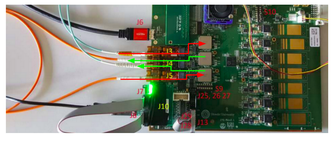

Figure 6: Long loopback test signal path.

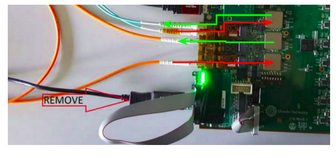

Figure 7: Short loopback test signal path.

- Slow-Controls Adaptor ADC (Analog-to-Digital-Converter) values are monitored to check rail voltages, temperatures, and other important values
- Functional tests are performed to check the functionality of LEDs, push-buttons, and switches
- Some of the temperature measurements on the boards need to be re-calibrated[Fig. 8]

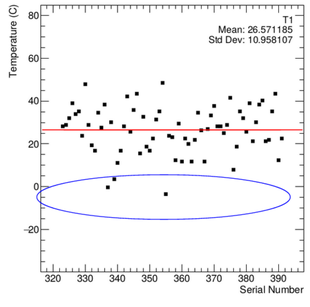

Figure 8: Temperature sensor tests showing out-of-range values.

Check and Fuse GBTx0

- Ensure configuration communication with all three GBTx's
- GBTx0 is fused with the necessary communication parameters
- GBTx1 and GBTx2 do not receive the golden fuse, and are re-programmed by the main FPGA during boot

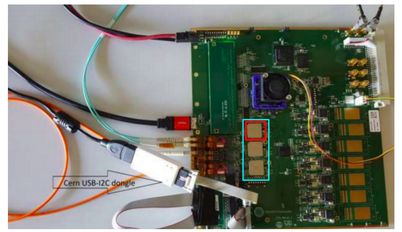

Figure 9: All three gigabit transceivers (GBTx), with GBTX0 highlighted in red.

Flash FPGA and CANbus Tests

- Flash FPGA must be re-programmed for detector use
- Test interface between the main FPGA and flash FPGA (select-map interface)
- Test interface between flash FPGA and flash memory (flash interface)
- Test slow controls adaptor communication
- Flash memory is mapped to locate all the bad blocks in order to avoid these during use

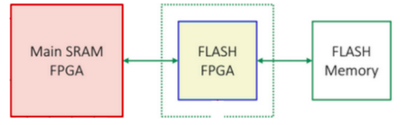

Figure 10: Graphic of the logic block, showing the interface between the three chips.

Conclusions

- Testing at Oak Ridge National Lab is going well and on-schedule
- 69 of 70 boards are currently functional, more than enough for detector commissioning
- Currently preparing a small experimental setup at ORNL that will simulate the full detector system