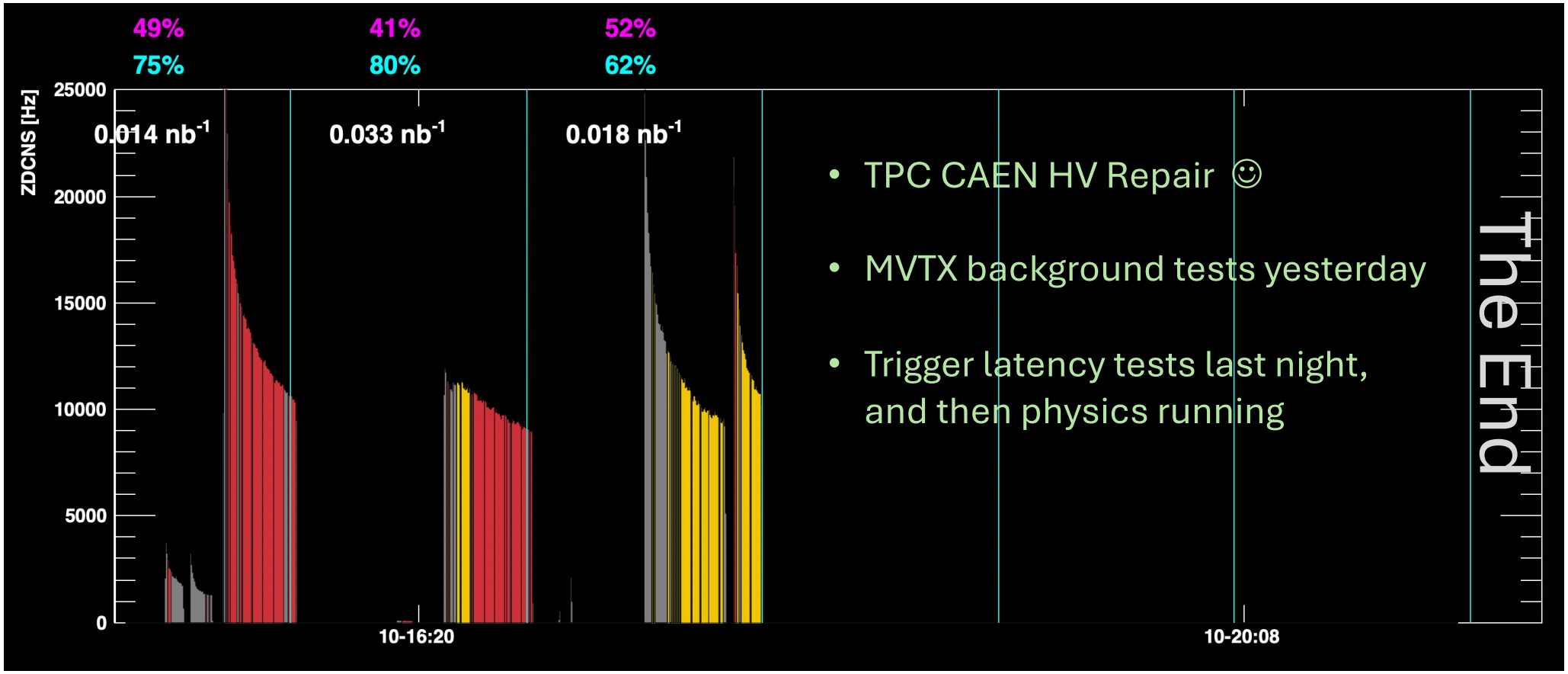
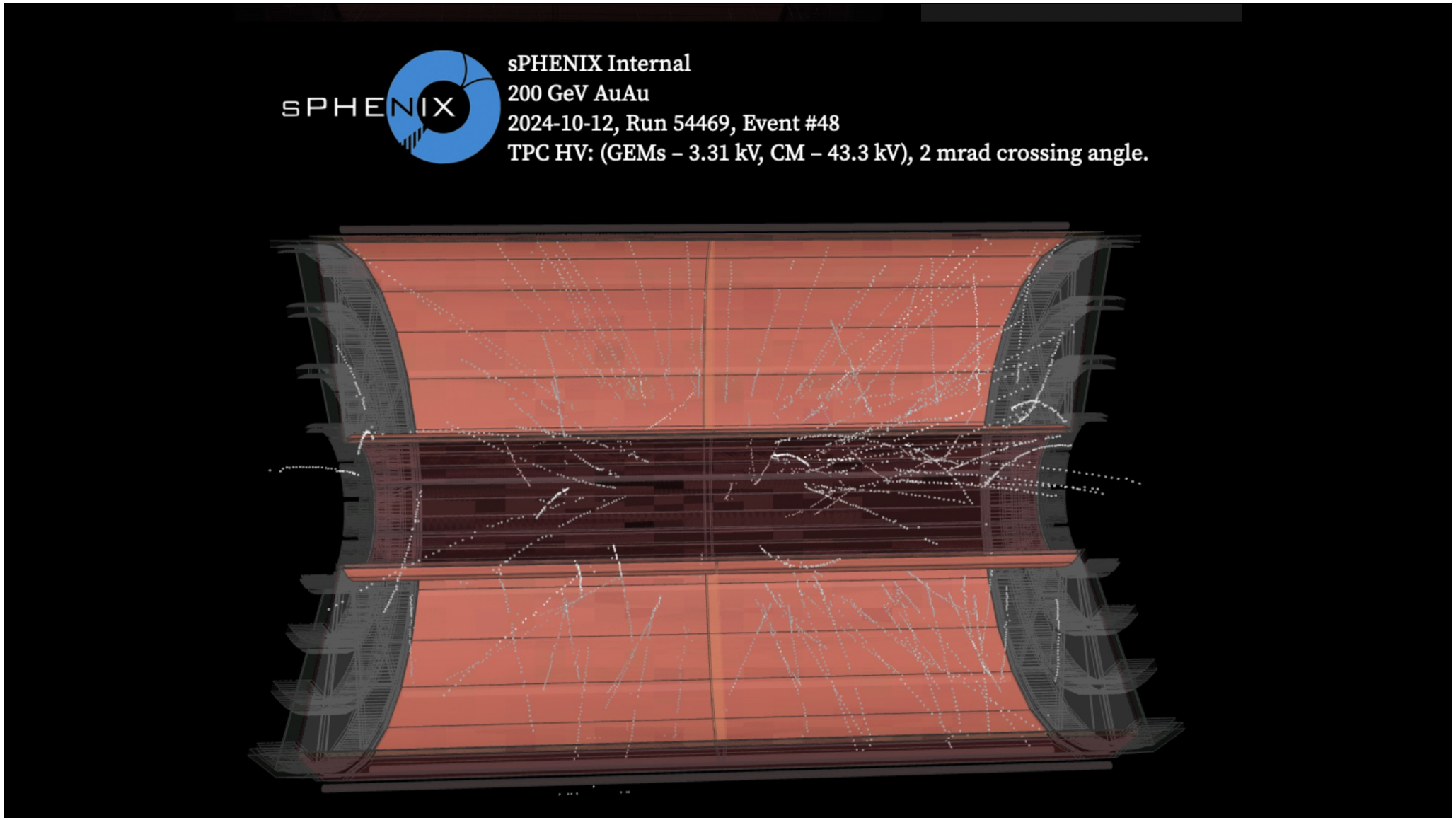
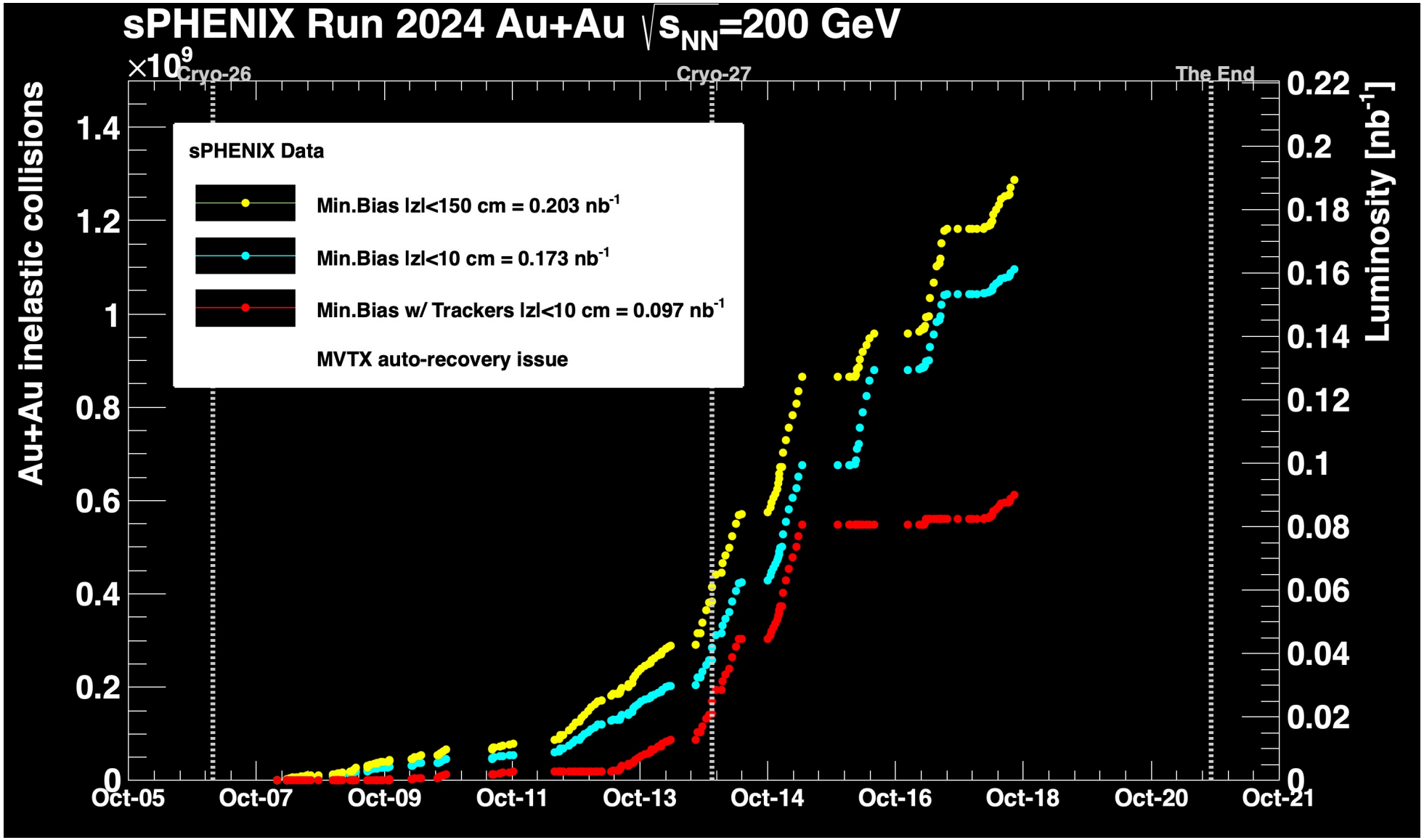
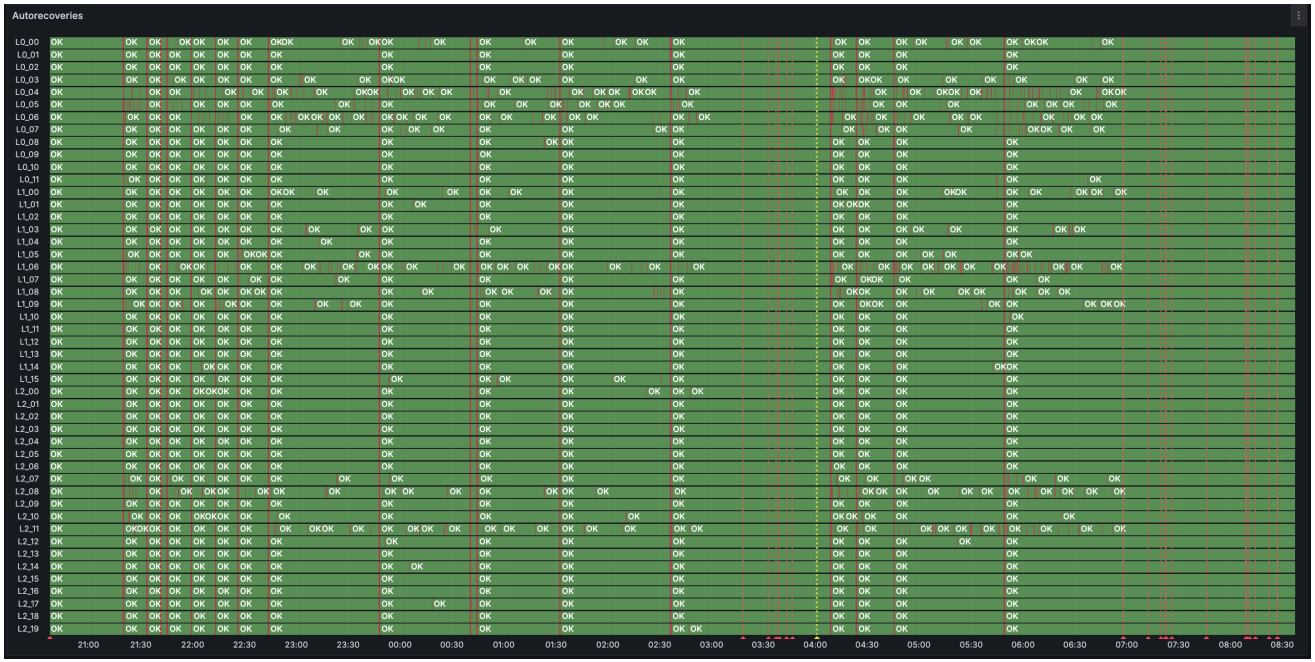


Tuesday Wednesday Thursday Friday Saturday Sunday


sPHENIX
sPHENIX Internal
200 GeV AuAu
2024-10-12, Run 54469, Event #48
TPC HV: (GEMs – 3.31 kV, CM – 43.3 kV), 2 mrad crossing angle.


sPHENIX Run 2024 Au+Au $\sqrt{s_{NN}}$=200 GeV
$\times 10^9$
Cryo-26
Cryo-27
The End
Au+Au inelastic collisions
Luminosity [nb^{-1}]
sPHENIX Data
Min.Bias |z|<150 cm = 0.203 nb^{-1}
Min.Bias |z|<10 cm = 0.173 nb^{-1}
Min.Bias w/ Trackers |z|<10 cm = 0.097 nb^{-1}
MVTX auto-recovery issue
0
0.2
0.4
0.6
0.8
1
1.2
1.4
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0.16
0.18
0.2
0.22
Oct-05
Oct-07
Oct-09
Oct-11
Oct-13
Oct-14
Oct-16
Oct-18
Oct-20
Oct-21

Last night – why were there so few auto-recoveries?



Of course, no auto-recoveries when we are not running ☺

sPHENIX was running a triggered mode test / latency scan.

MVTX – design in sPHENIX to run in streaming mode with 5-10 microsecond strobe. In that case, 100% of "big splash" events will cause an auto-recovery.

If we can run in triggered mode (which is supported), the auto-recoveries will only be if there is a "big splash" event coincident with a triggered event within 5 microseconds.

Thus, if we run the DAQ rate at 2 kHz, one only sees 2e3 x 5e-6 = 1% of "big splash events", and so auto-recovery rate is expected to be **100x** lower.

The sPHENIX Au+Au plan is for a DAQ rate of 15 kHz, which still should reduce the auto-recovery rate by **13x**.

This effort is completely multiplicative in benefit to any reduction in the "big splash" event rate by C-AD.

What is the challenge of running the MVTX in triggered mode?

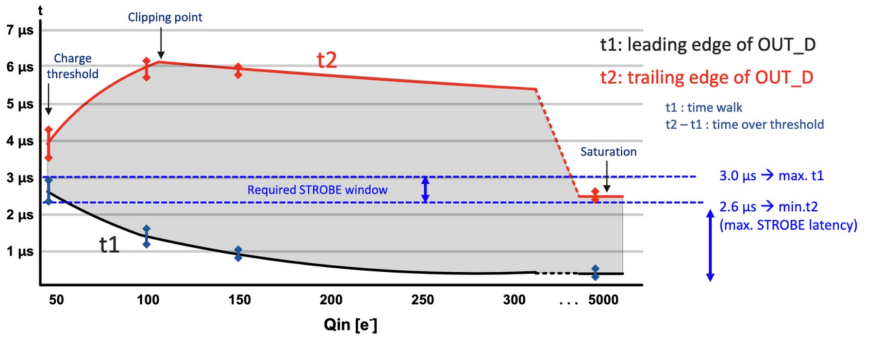
sPHENIX was designed with 4 microsecond trigger latency spec.

The graph below shows that this is late for the ALPIDE chip and will miss hits,

And this will be charge-deposit dependent.

Timing of Discriminator Output

ALICE



t1: leading edge of OUT_D

t2: trailing edge of OUT_D

t1 : time walk

t2 – t1 : time over threshold

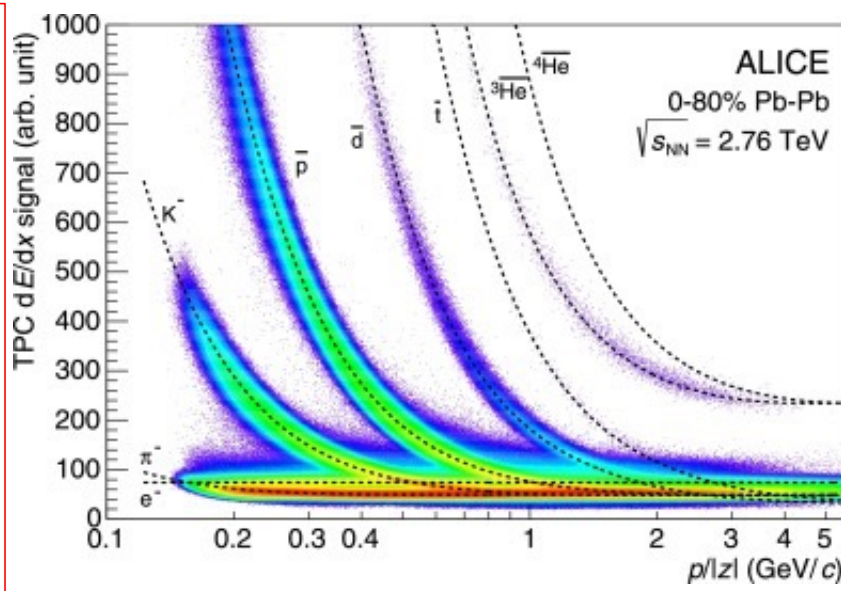
3.0 µs → max. t1

2.6 µs → min.t2 (max. STROBE latency)

Q_{in}	t1 [us]	t2 [us]
50 e⁻	2.9 ±0.20	3.9 ±0.52
100 e⁻	1.5 ±0.16	5.9 ±0.24
150 e⁻	0.9 ±0.03	5.7 ±0.09
5 ke⁻	0.5 ±0.01	2.6 ±0.07

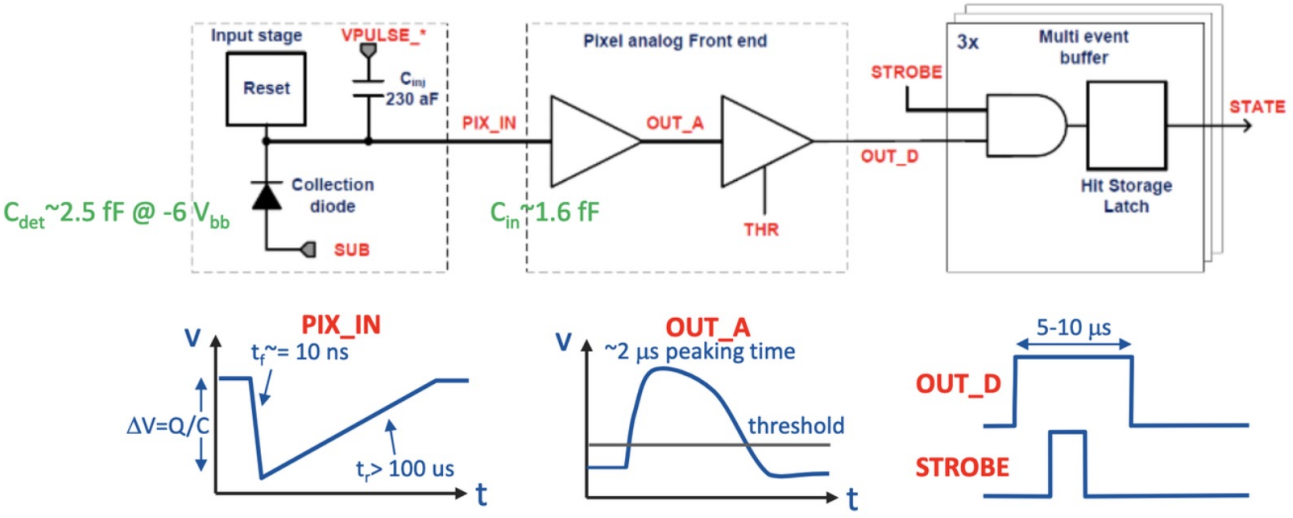
Simulation results

SOURCE: ALPIDE CHIP Production Readiness Review



Charge deposit depends on particle momentum and species. Note that heavy flavor decays include kaons and protons.

Pixel



Analog front-end and discriminator continuously active

- Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
- The front-end acts as analogue delay line
- Test pulse charge injection circuitry
- Global threshold for discrimination -> binary pulse OUT_D

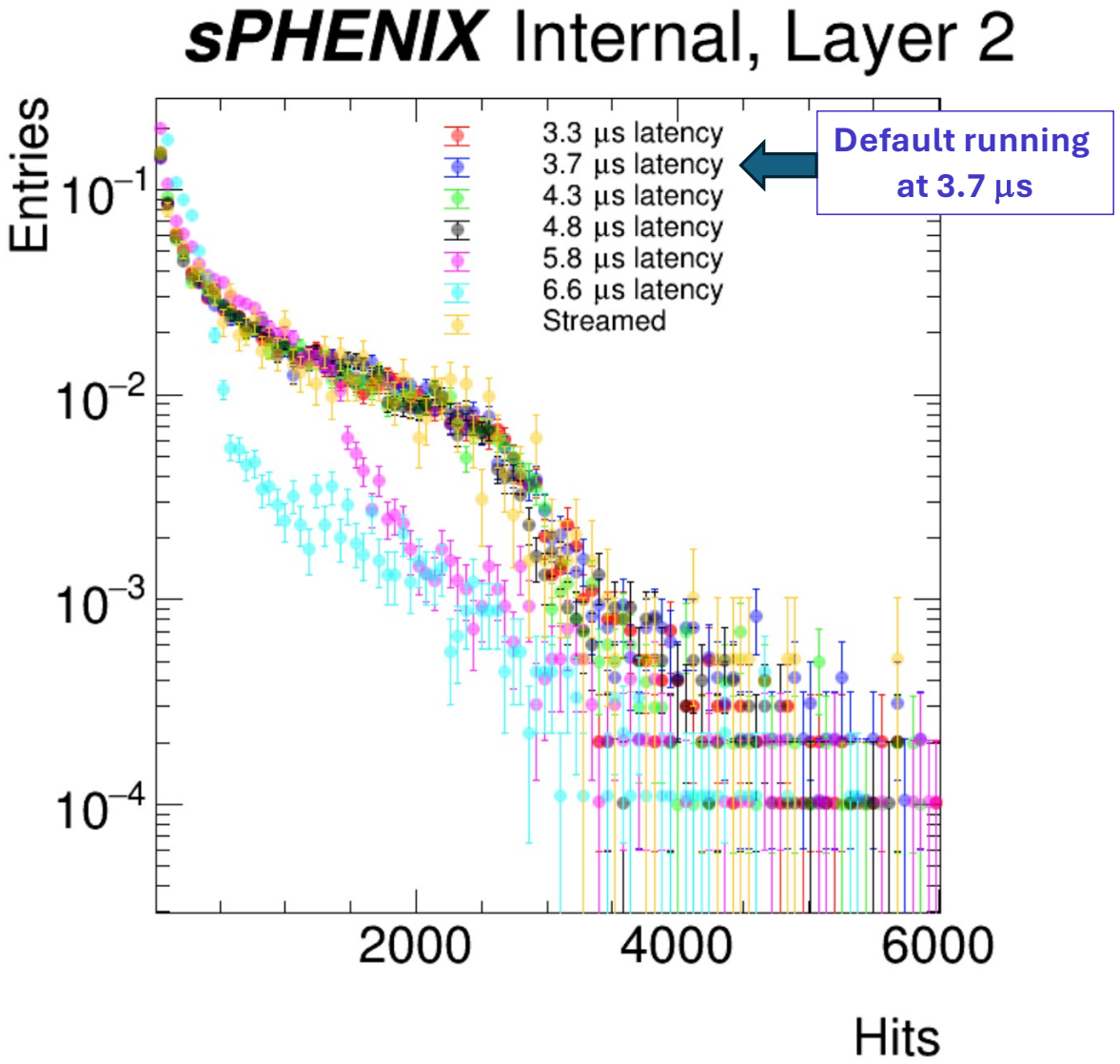
Front End Characteristics (Simulated)	
Gain (small signal) [mV/e]	4
ENC [e]	3.9
Threshold [e]	92 ± 2

Digital pixel circuitry with three hit storage registers (multi event buffer)

- Global shutter (STROBE) latches the discriminated hits in next available register
- In-Pixel *masking* logic

This is a good sign, but again, we need a full analysis with offline tracking (MVTX, INTT, TPC) to understand if efficiency for low momentum kaons and protons is lower...

Also, we request 5 hours of a 12x12 stable store either tonight or tomorrow overnight. Key for TPC checks.



sPHENIX End-of-Gold Party

Monday, October 21, 2024
noon

Come one, come all...
to the sPHENIX parking lot.
Food and beverages
(and cake) will be served.