ALICE-USA
BTU Project

BTU TPC Electronics WBS 1.1.2

C. L. Britton

K. F. Read

D. Simpson

Oak Ridge National Laboratory and

University of Tennessee

ALICE-USA
BTU Project

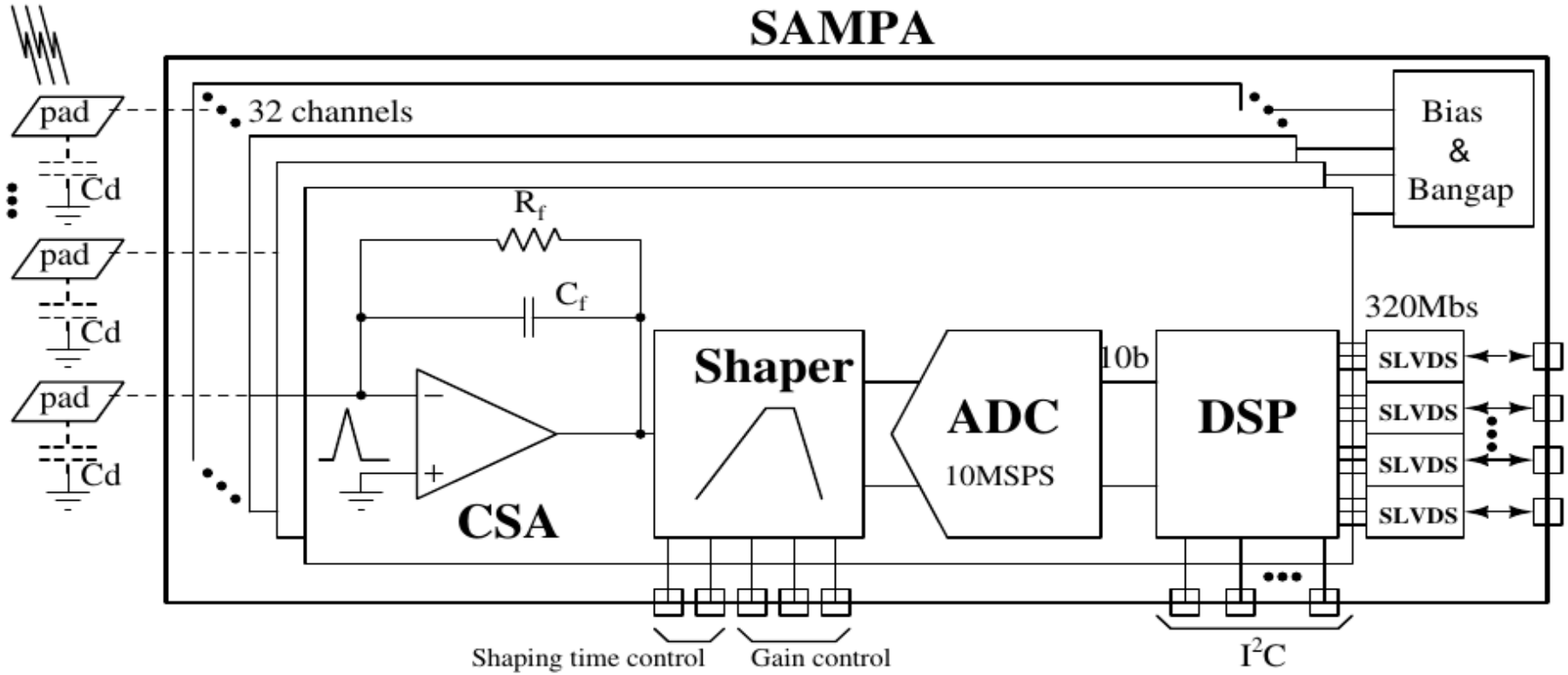
Outline of the talk

- SAMPA
  - MPW1 tests
  - MPW2 plan
  - MPW2 status
- FEC Design
  - Final architecture
  - Prototype stages
  - Rev0 status

SAMPA

ALICE-USA
BTU Project

SAMPA Block Diagram



ALICE-USA
BTU Project

SAMPA Readout ASIC

- Designed at University of Sao Paulo, Brazil
- Process is 0.13um TSMC
- This is a common ASIC to be used within ALICE by both TPC and MCH.
- Chip has 311 pins.
- Final package will be a 372-Ball Grid Array (BGA)

(80 ns peaking removed)

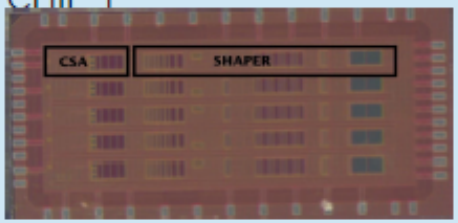
Specification	TPC	MCH
Voltage supply	1.25V	1.25V
Polarity	Positive/Negative	Positive/Negative
Detector capacitance (Cd)	18.5pF	40pF - 80pF
Peaking time (ts)	~~80ns or~~ 160ns	300ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	~~< 536e@ts=80ns*~~ or < 482e@ts=160ns*	< 950e @ Cd=40p* < 1600e @ Cd=80p*
Linear Range	100fC or 67fC	500fC
Sensitivity	20mV/fC or 30mV/fC	4mV/fC
Return to baseline time	~~<164ns@ts=80ns~~ or <288ns@ts=160ns	<541ns
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=80ns or < 0.2%@ts=160ns	< 0.2%@ts=300ns
ADC effective input range	2Vpp	2Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10Msamples/s or 20Msamples/s	10Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
SFDR (ADC)**	68dBc	68dBc
SINAD (ADC)**	57dB	57dB
ENOB (ADC)	< 9.2-bit	< 9.2-bit
Power consumption (per channel) ADC CSA + Shaper	 2mW (4mW) 6mW	 2mW (4mW) 6mW
Channels per chip	32	32

SAMPA MPW1 Tests

Chips fabricated on the MPW1

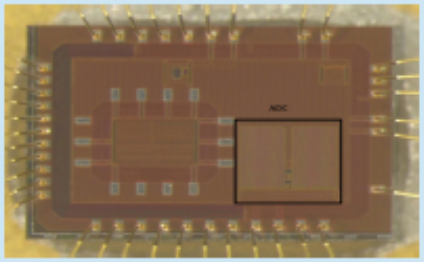
Chips fabricated: MPW1 (blocks testing)

CHIP 1



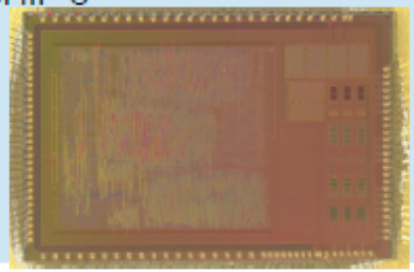
5 channel of the front-end:
CSA + Shaper+Bias

CHIP 2



ADC + SLVDS drivers (Receiver and Transmitter)

CHIP 3

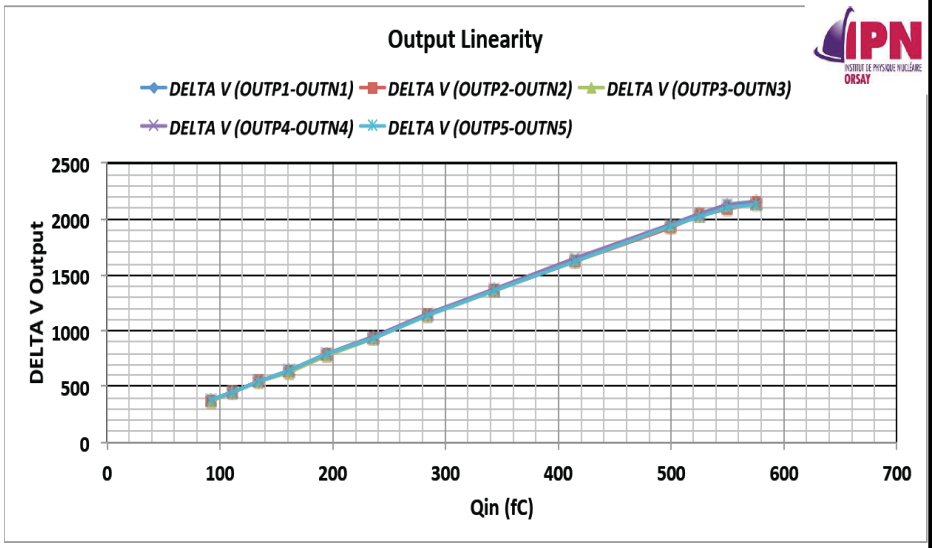


Front-end + ADC + DSP + Circuits for testing

ALICE-USA
BTU Project

MPW1 Linearity

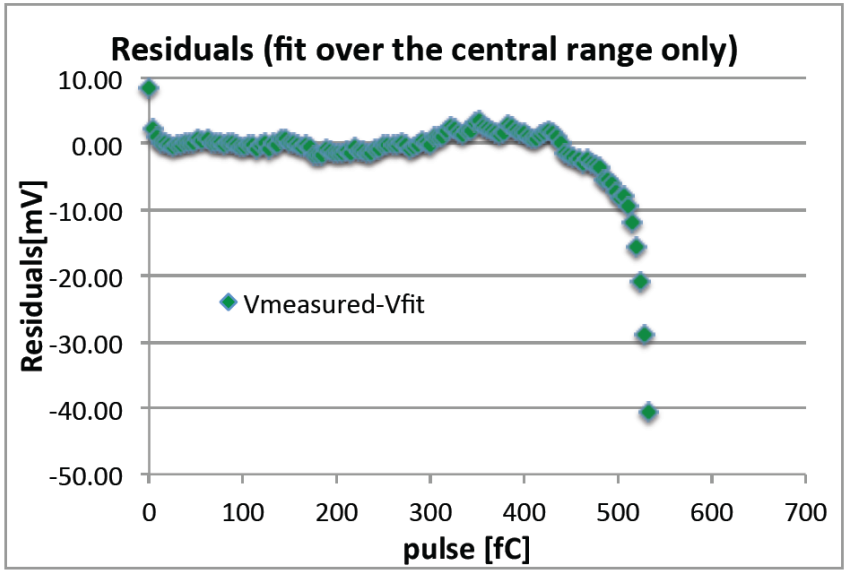
Chip1: Gain value [4mV/fC Pos]



Constant slope up above 500fC pulsed

Chip1: Gain linearity [4mV/fC Pos]

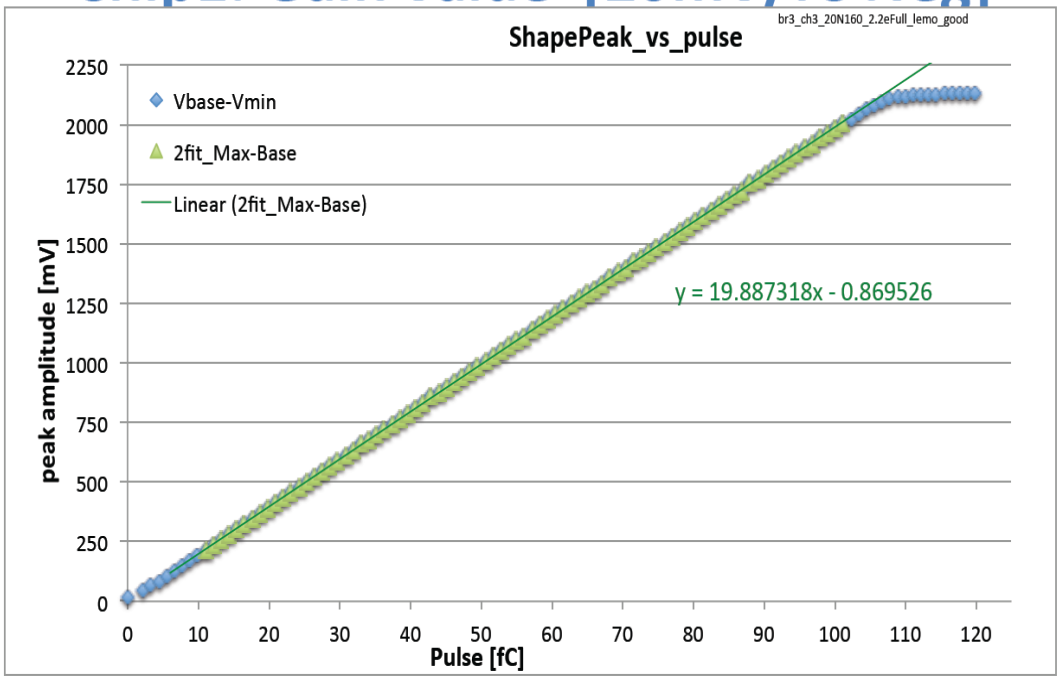
(different chip/lab)



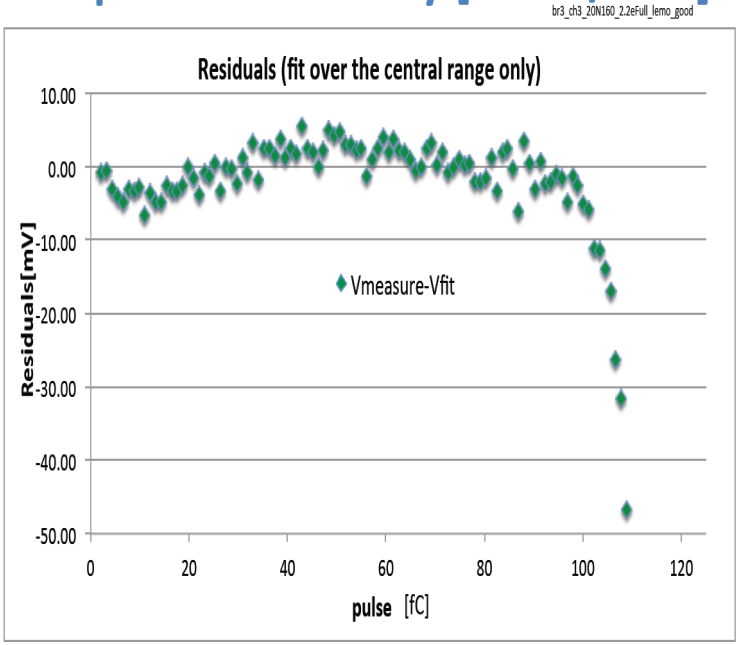
ALICE-USA
BTU Project

MPW1 Linearity

Chip1: Gain value [20mV/fC Neg]

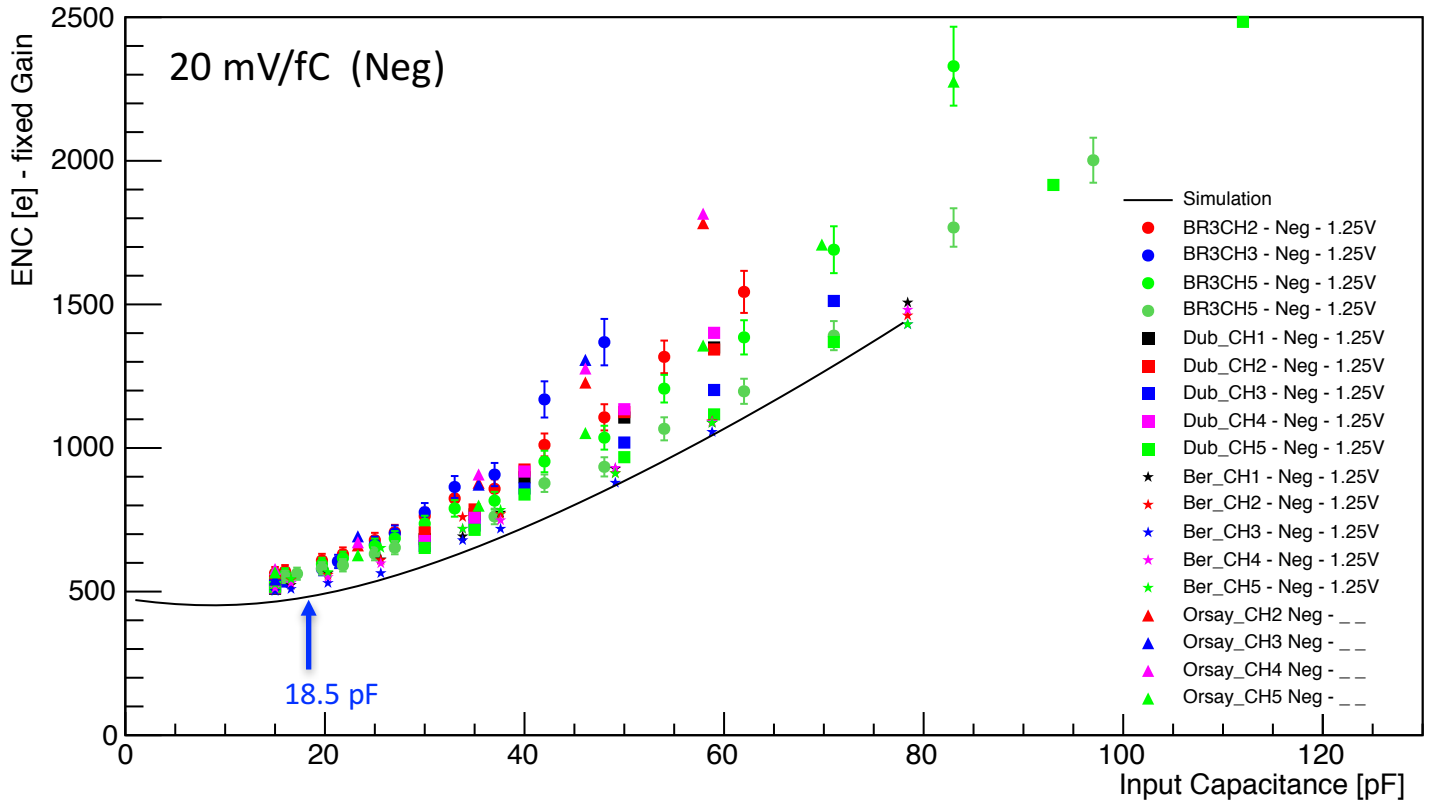


Chip1: Gain linearity [20mV/fC N]

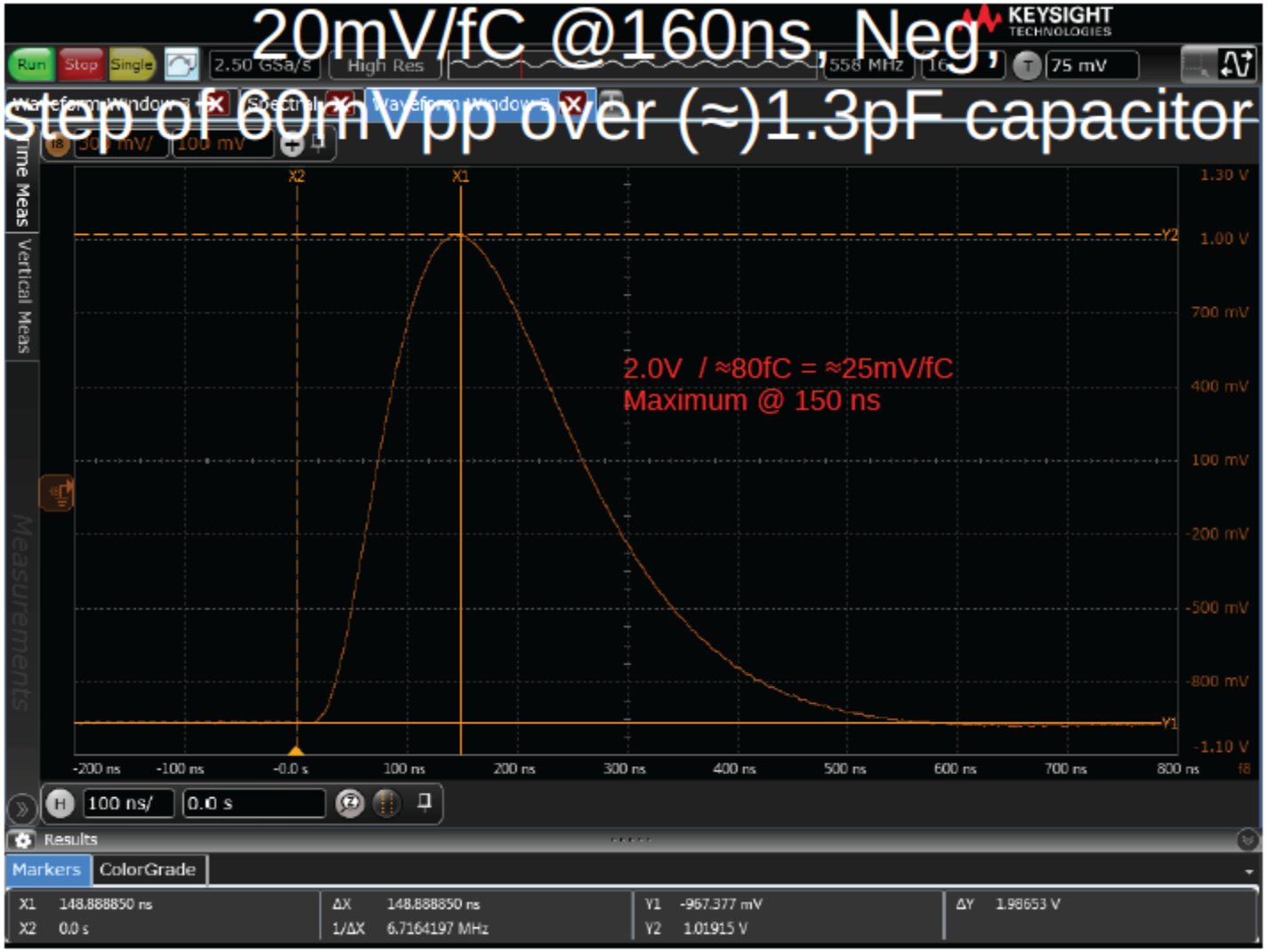


ALICE-USA
BTU Project

MPW1 Noise



TPC Shaping time measurement

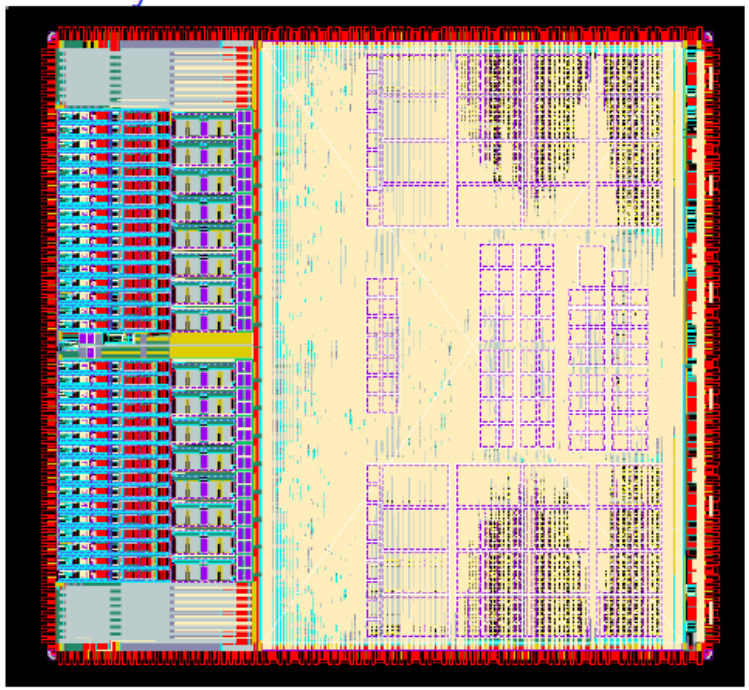


SAMPA MPW2

SAMPA MPW2 consists of several ASICs

- Includes the full 32 channel ASIC
- Test chip 01
  - Full shaper
  - SLVS TX/RX
  - Bias
- Test chip 02
  - 32 channel CSA/Shaper/buffer
- Test chip 03
  - ADC

Full Layout

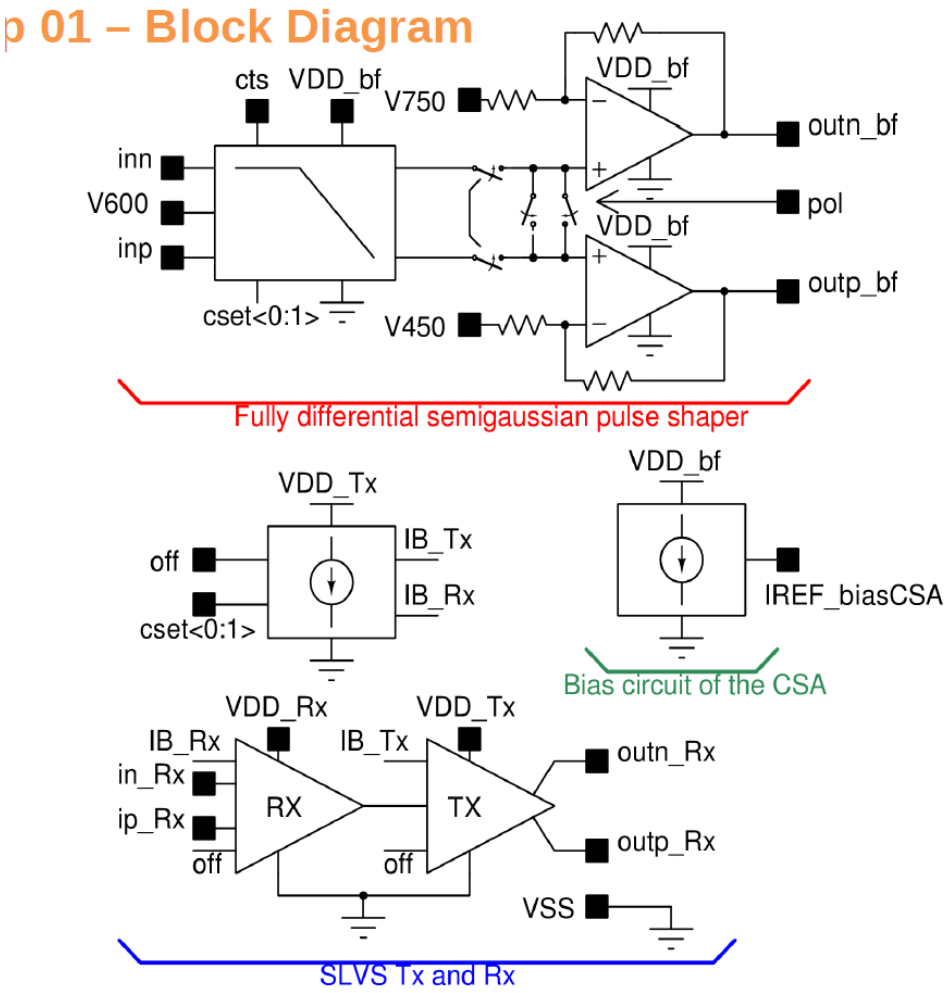


Die size - 9533.6um x 8943.6um

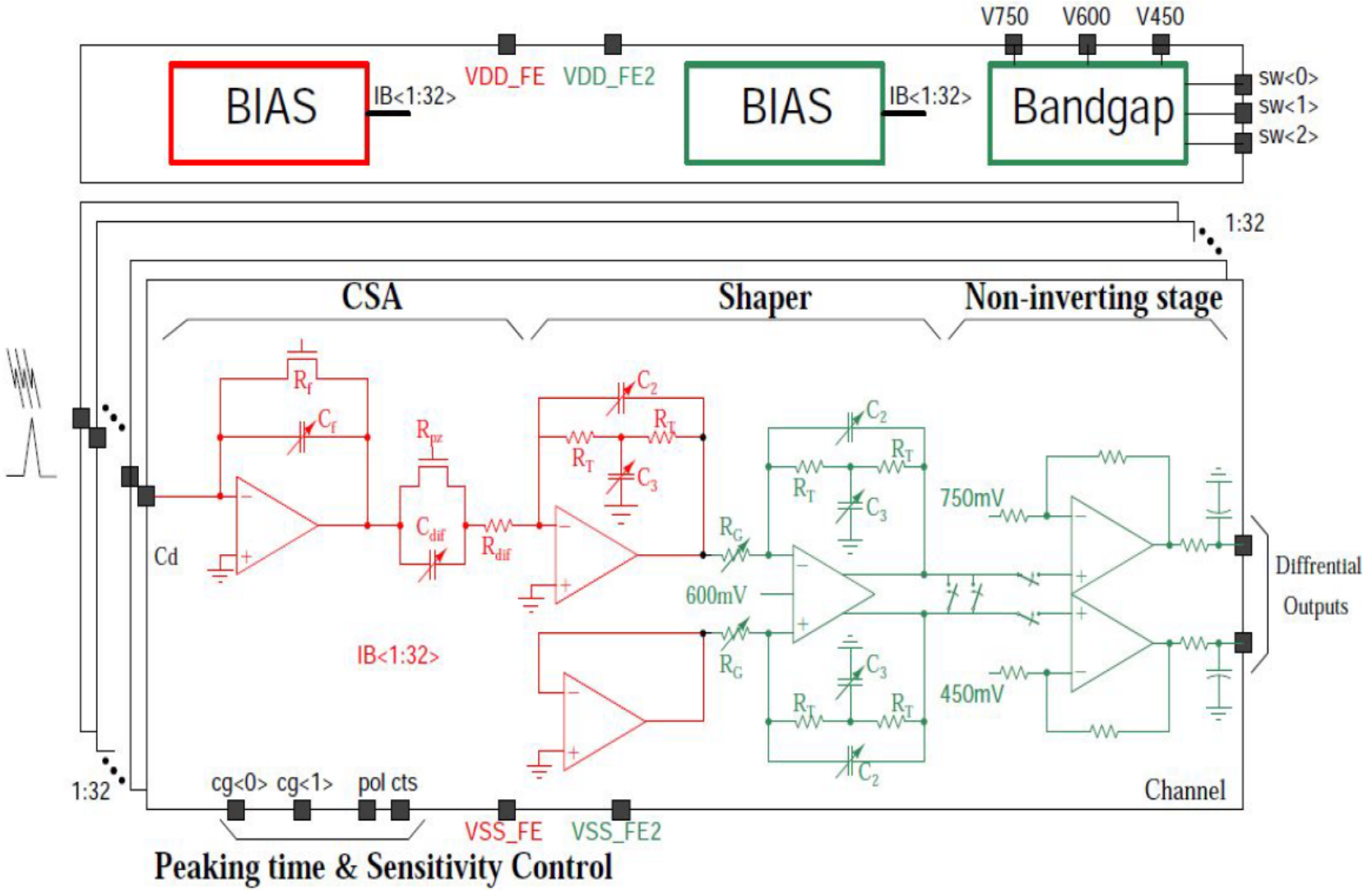
Pin count – 311, Ball count - 372

ALICE-USA
BTU Project

Test chip 01

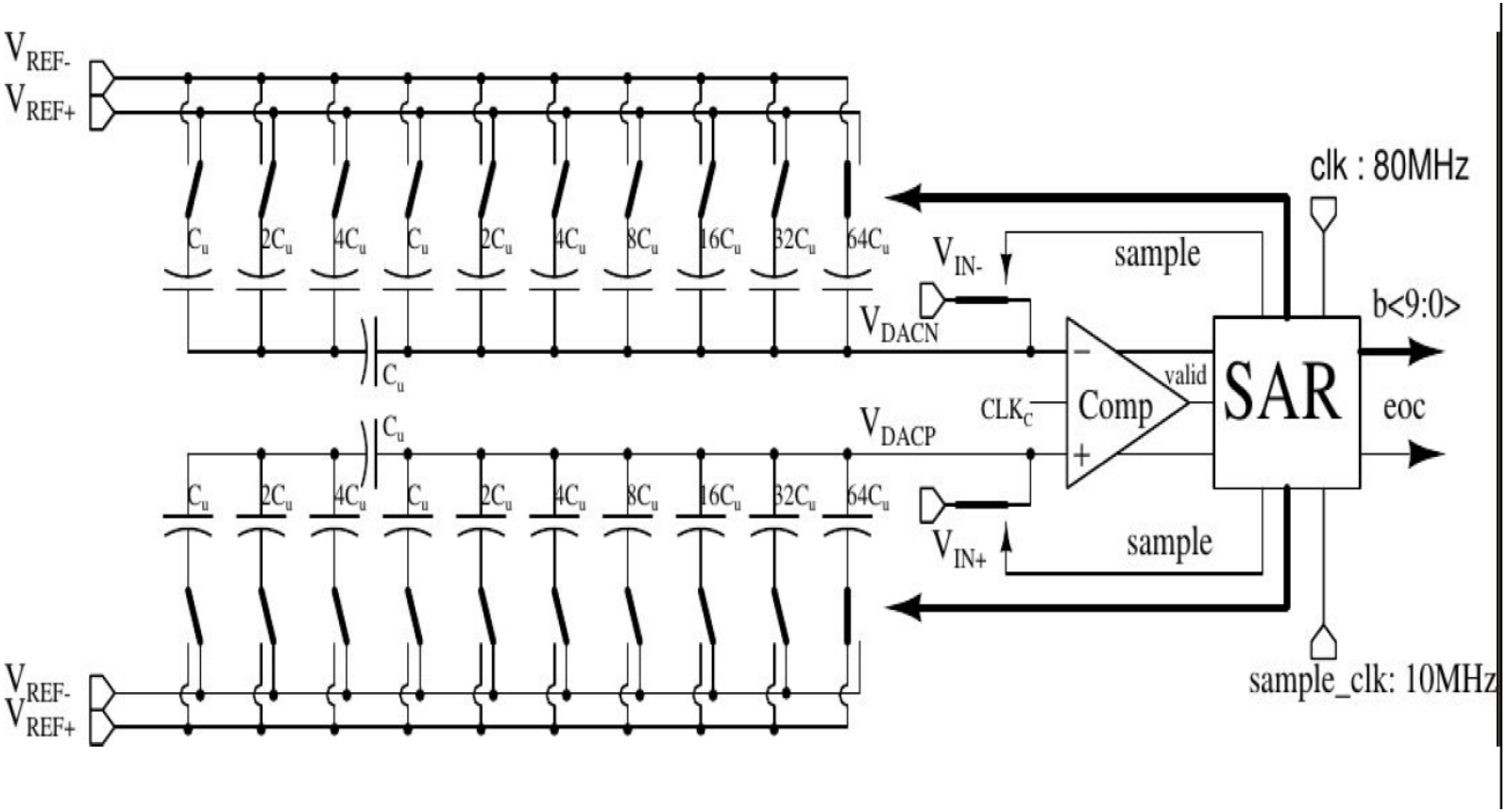


Test chip 02


V750
V600
V450
BIAS
IB<1:32>
VDD_FE
VDD_FE2
BIAS
IB<1:32>
Bandgap
sw<0>
sw<1>
sw<2>
1:32
CSA
Shaper
Non-inverting stage
Cd
750mV
600mV
450mV
IB<1:32>
Diffrential
Outputs
1:32
cg<0>
cg<1>
pol
cts
VSS_FE
VSS_FE2
Channel
Peaking time & Sensitivity Control

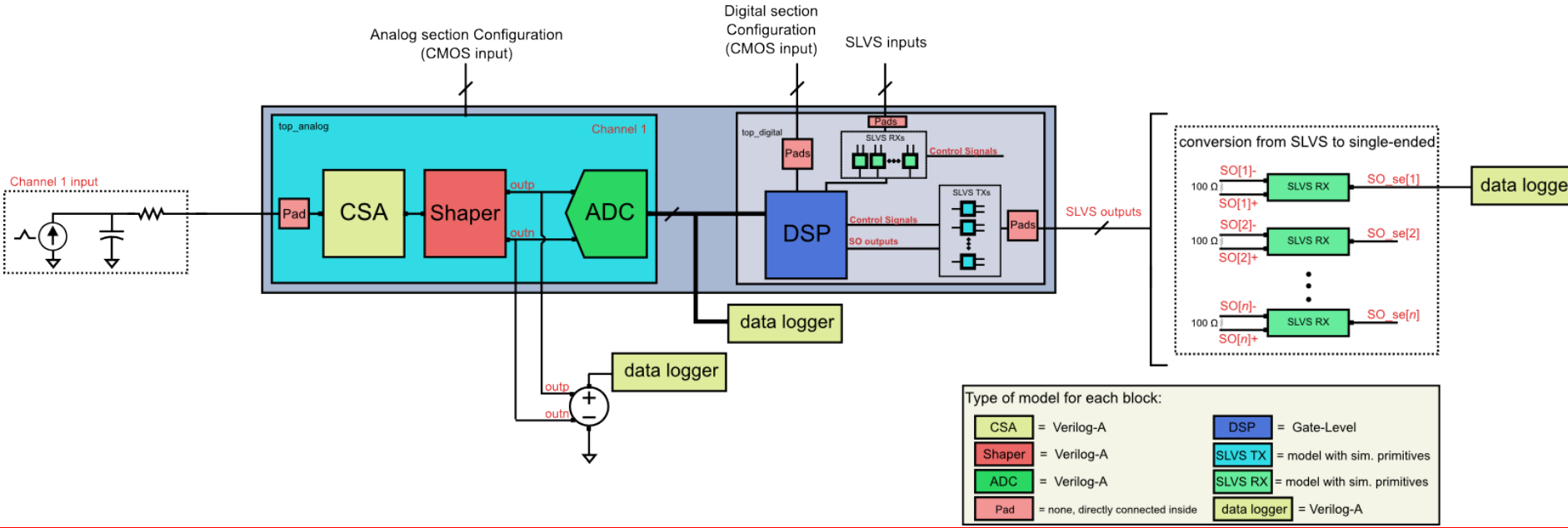
ALICE-USA
BTU Project

Test chip 03



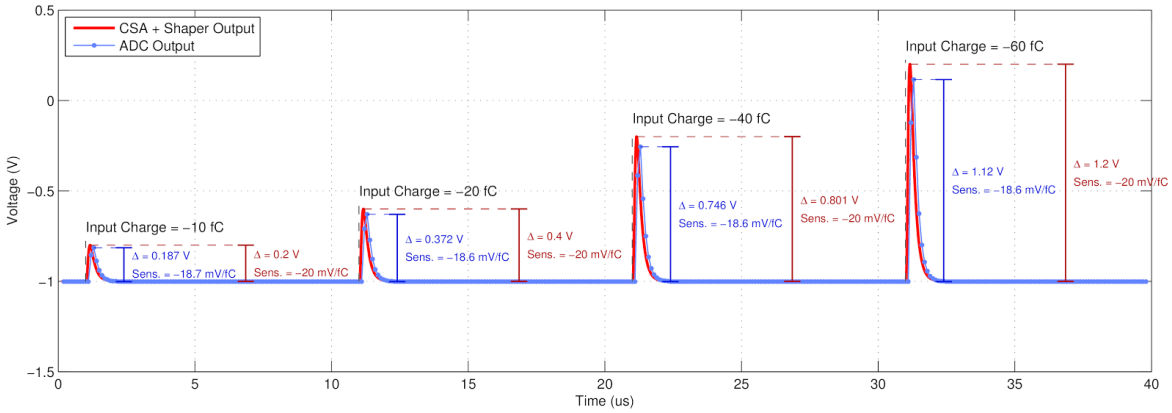
SAMPA Simulation

- A full suite of simulations were done in various domains
- Due to computing limitations, the entire chip was not simulated as a single entity
- The MPW2 analog section had extensive oversight and rigor with review and monitoring by ALICE, CERN, and ORNL reviewers.
  - Appropriate due diligence exercised for design.
  - Extensive, superior simulations were performed.
  - Multiple testbenches used to check digital control functionality.

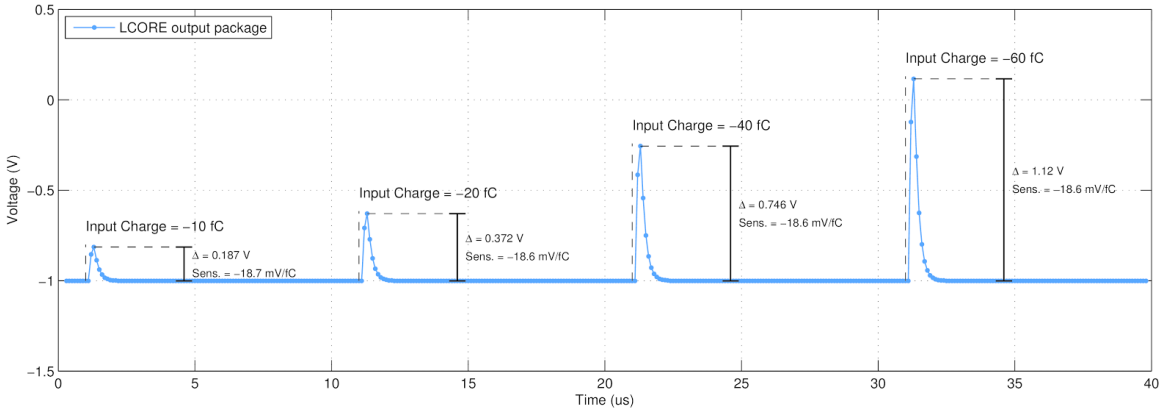


Front-end plus ADC simulations (cont.)
(Neg pol., 20mV/fC, 160ns)

Mixed-signal Simulation.



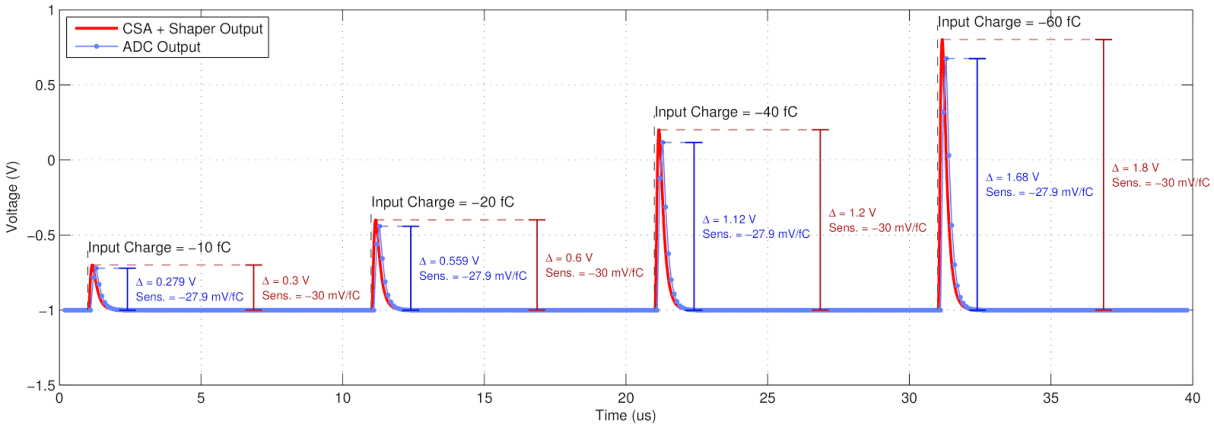
Top-level digital output. Fit included.



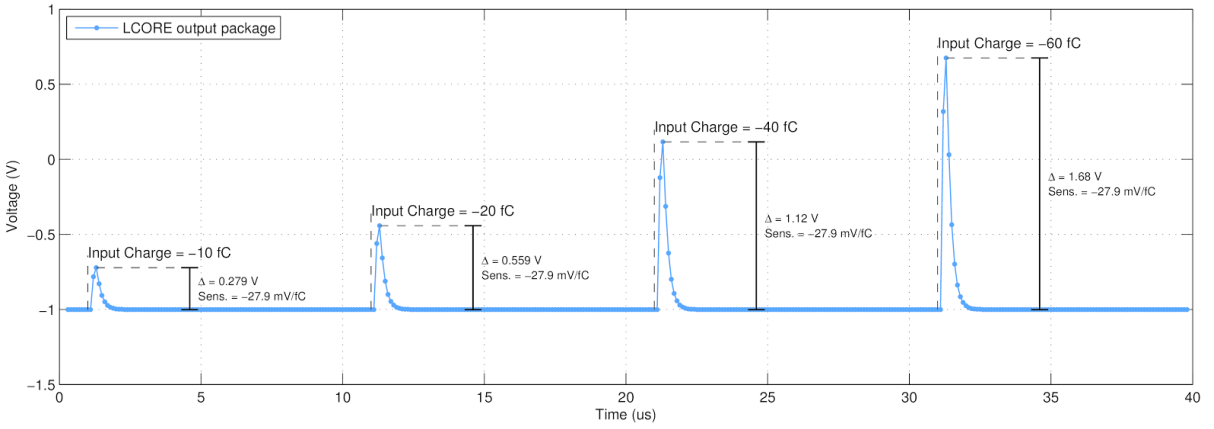
Front-end plus ADC simulations

(Neg pol., 30mV/fC, 160ns)

Mixed-signal Simulation.



Top-level digital output. Fit included.



Noise Simulations

Configuration of the simulation

- "Transient" noise channels 1,3,5,7
- 1500 point, 5 ns step, 7.5µs simulated signal
- VDD=1.25
- Cd=Typical
  - MCH -> 40 pF
  - TPC -> 18.5 pF
- Lb=4nH/wire

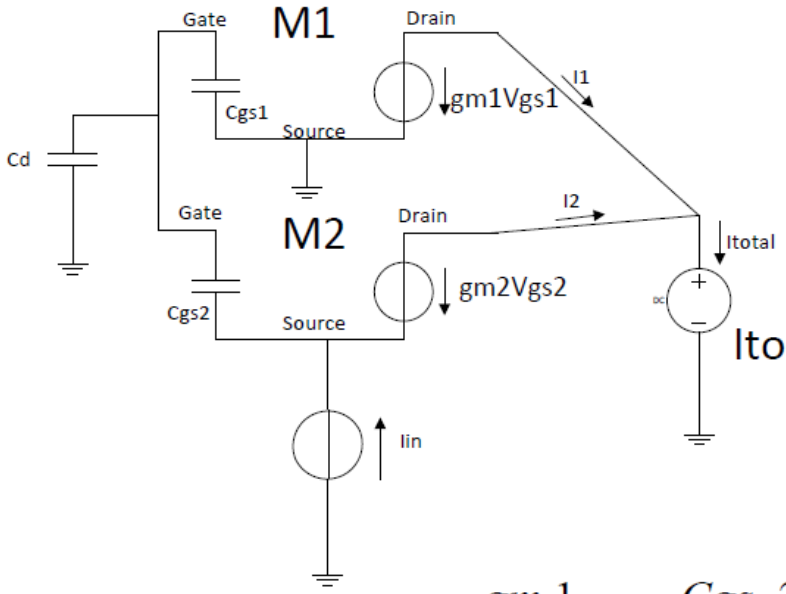
SUMMARY TABLE

Conf	Gain [mV/fC]	noise [mVrms]	enc
4mV_pos	4	0.84	1305
20mV_pos	20	1.5	466
20mV_neg	20	1.507	468
30mV_pos	30	2.162	448
30mV_neg	30	2.169	449

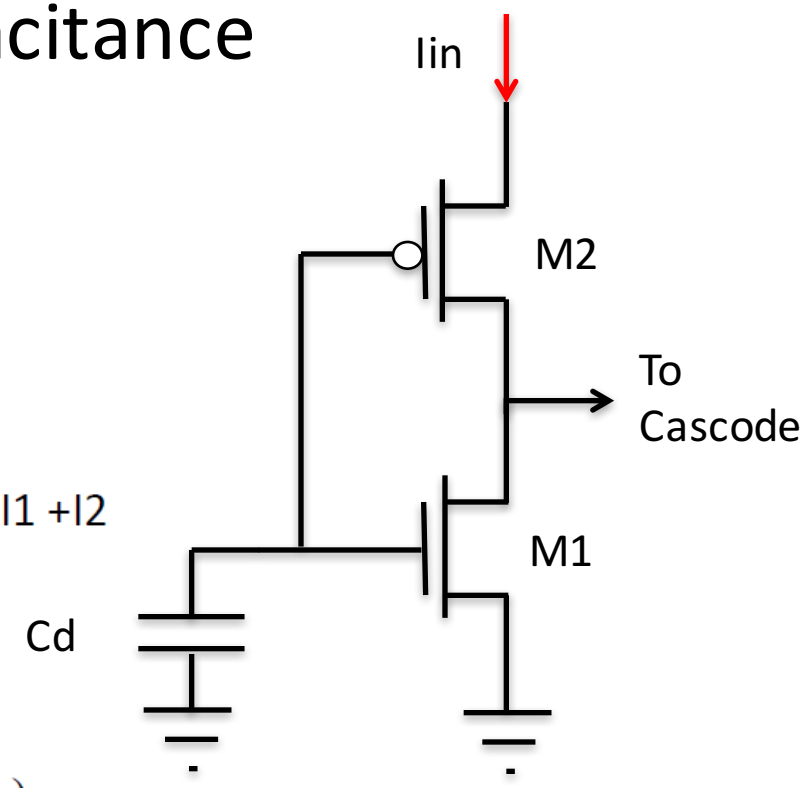
No visible difference among the 4 channels simulated (1,3,5,7)

Noise ~ gausssian for 20&30 confs, ENC value OK
Noise "strange" for 4mV conf. ENC value high, investigating.

The preamp noise can be optimized at a single detector capacitance



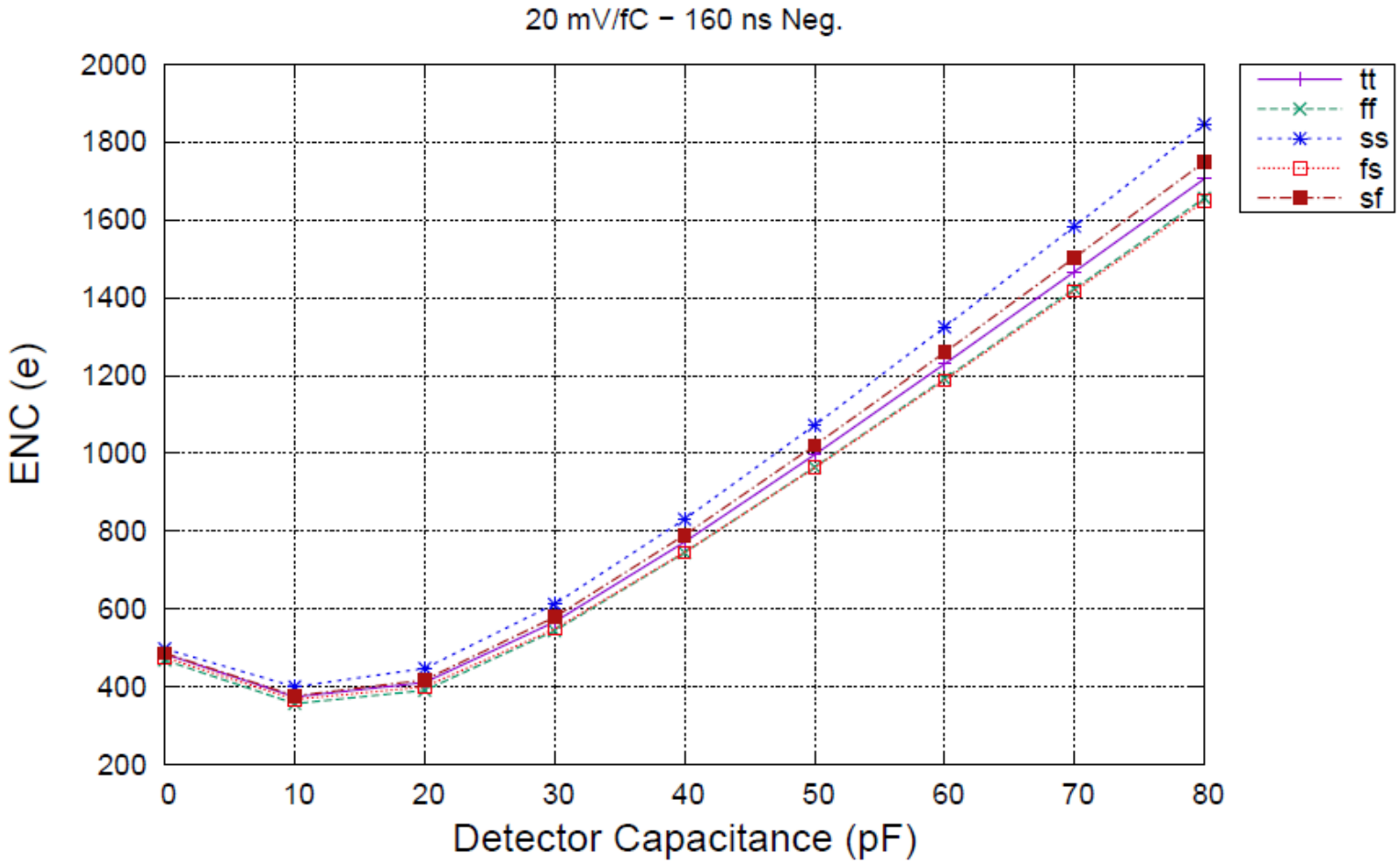
Itotal=I1 +I2



$$\frac{Itotal}{Iin} = \frac{1 - \frac{gm\ 1}{gm\ 2}\left(\frac{Cgs\ 2}{Cd\ + Cgs\ 1}\right)}{1 + s\frac{Cgs\ 2}{gm\ 2}}$$

Improves noise due to both drain-bias transistor and power-supply

Noise Simulation (cont.)

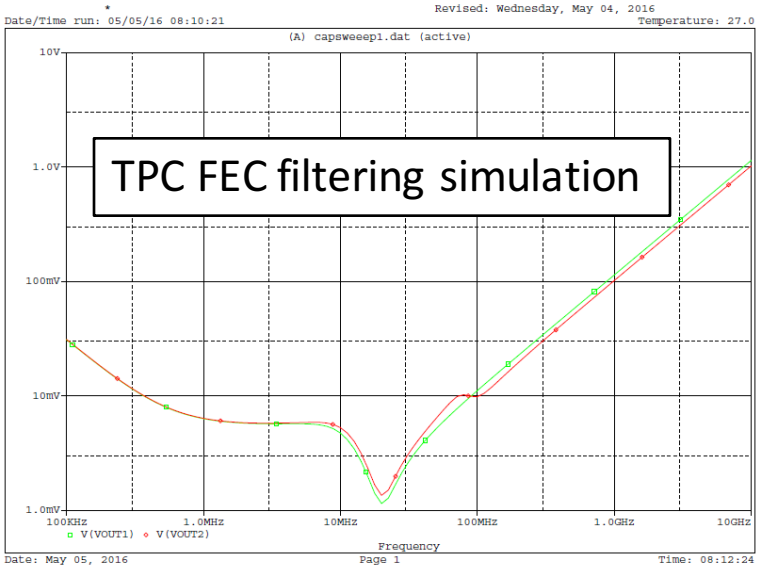


ALICE-USA
BTU Project

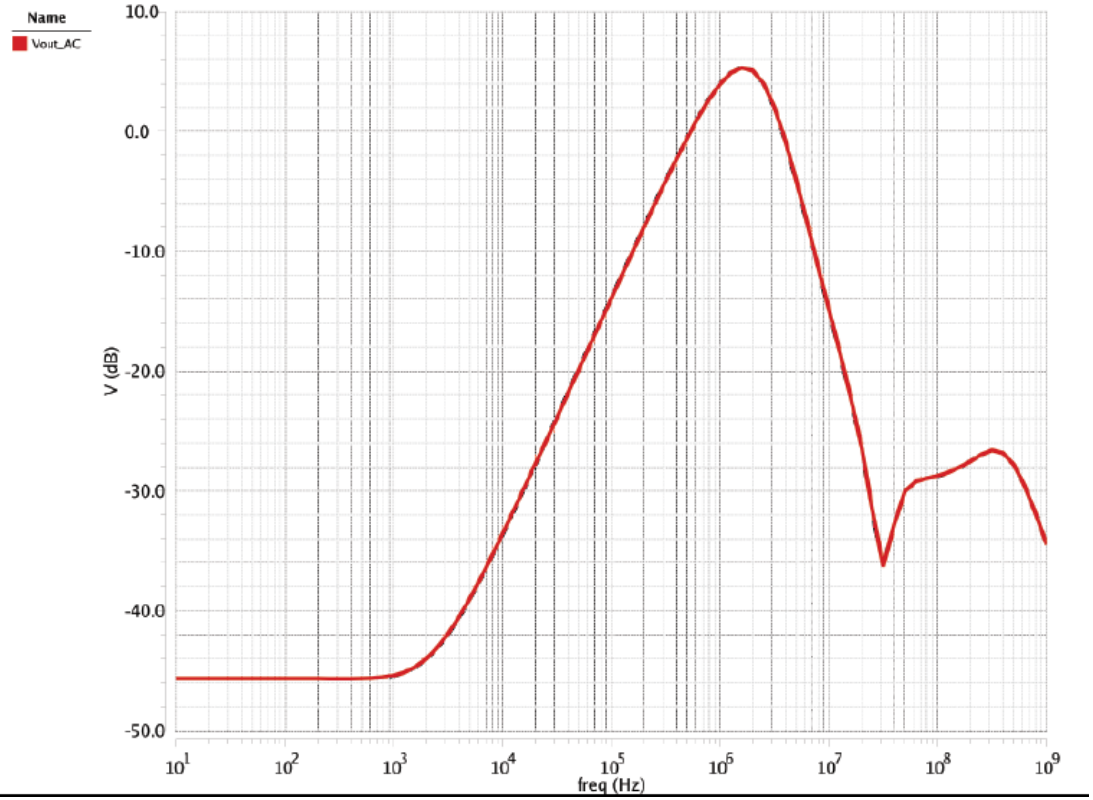
PSRR Simulations

Conditions

- DC+perturbation injected on all VDD pads
- Read ch8 Front-End output (output of the 2nd shaper)
- Extracted simulation
- PSRR= 20*log10(Vout_AC / VDD_AC)

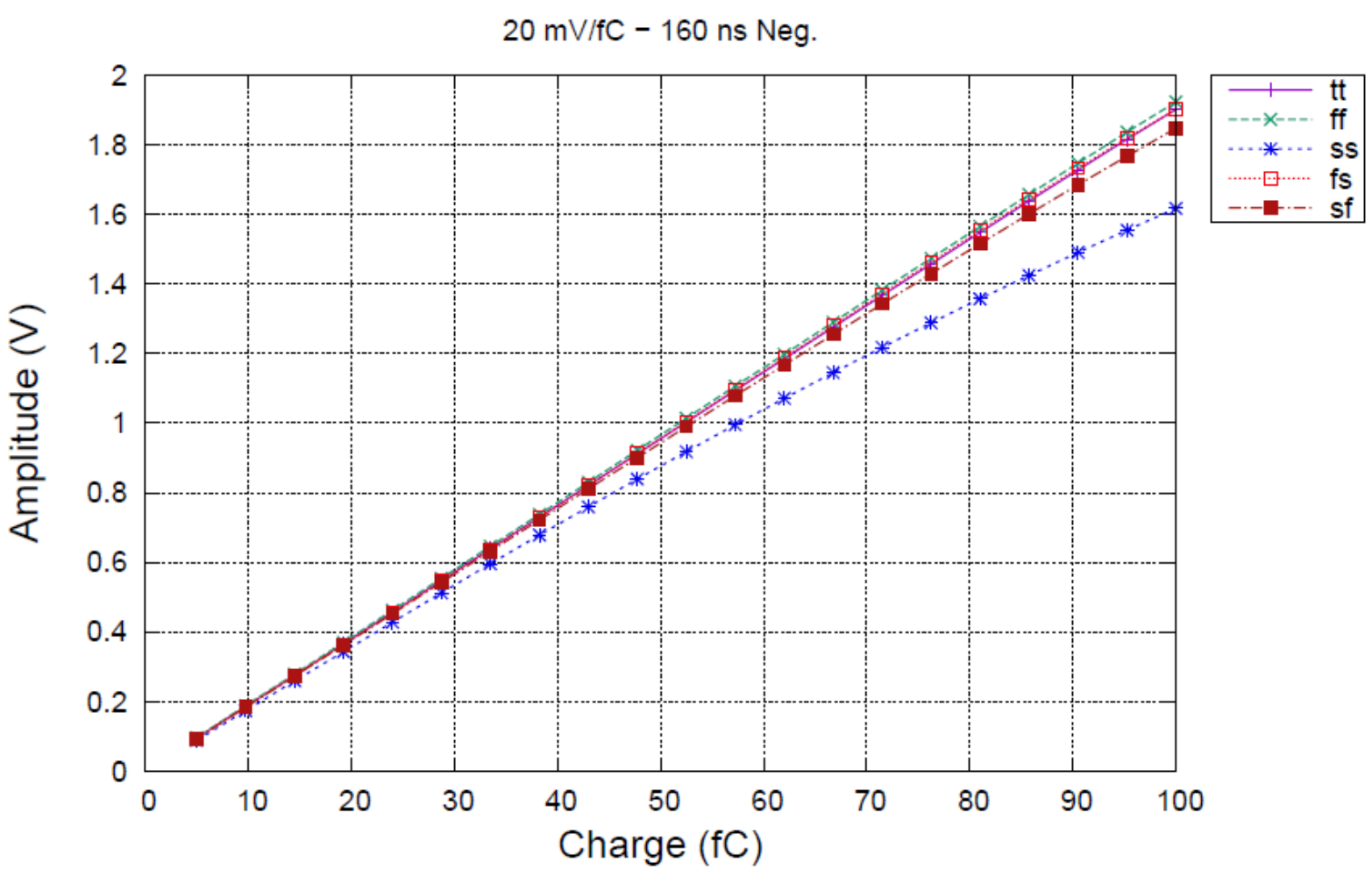


20mV/fC neg (VDD 1.25V)



ALICE-USA
BTU Project

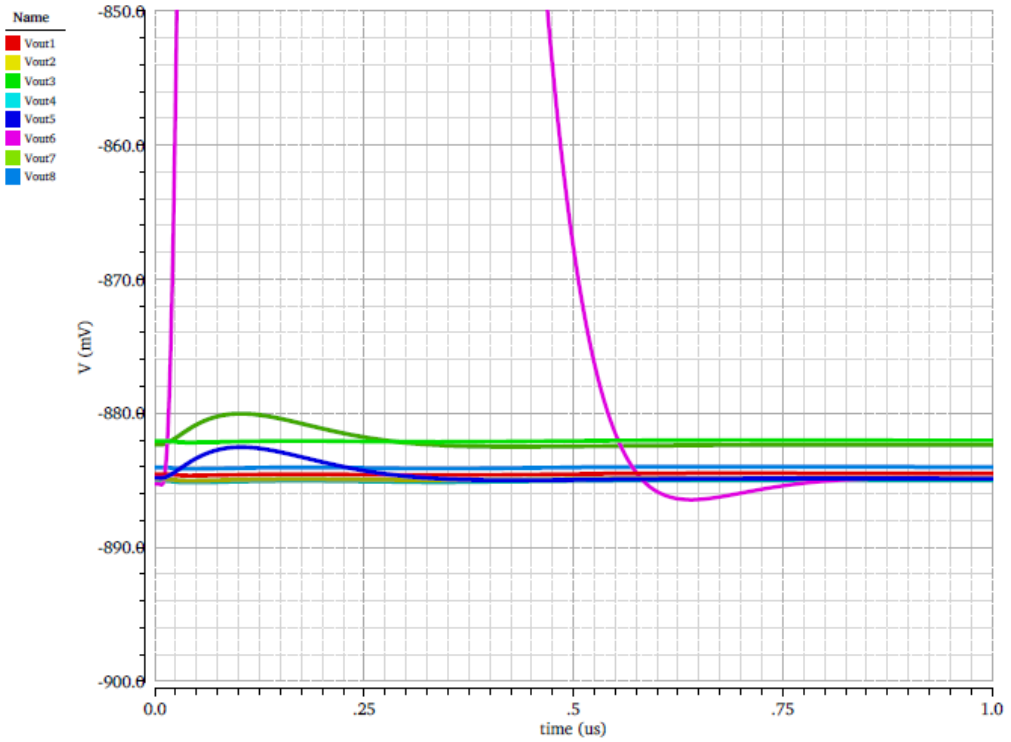
Linearity simulations (postlayout)



Crosstalk simulations

xtalk 20mVneg 50fC VDD119 MinCD; pulsed channel :6

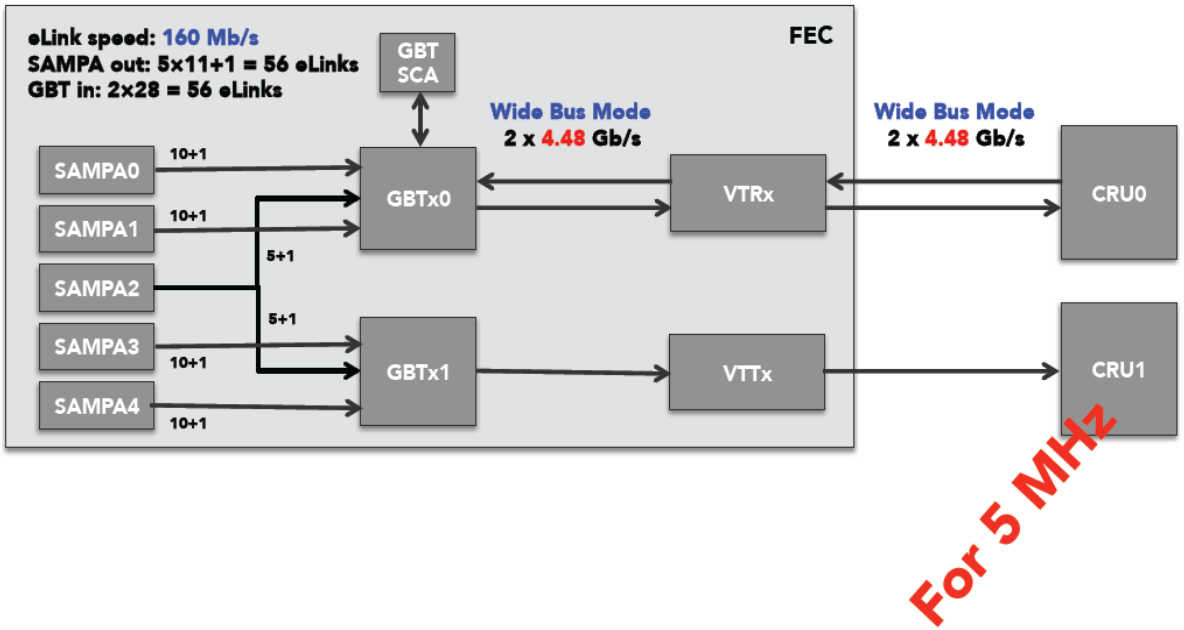
- Signal due to crosstalk in adjacent channel less than ~0.25%
- No crosstalk appears in second channels



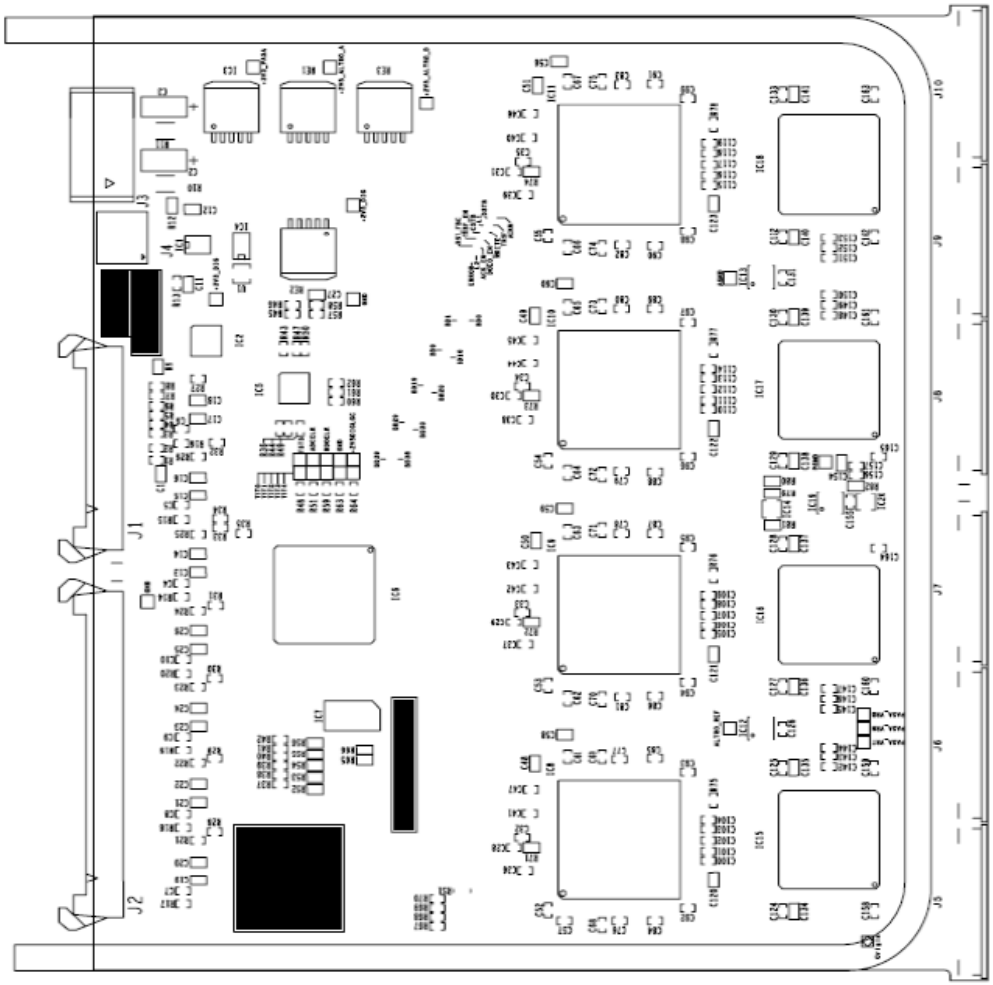
FEC Design

TPC FEC Final Readout Architecture

TPC FEC with 5 MHz sampling

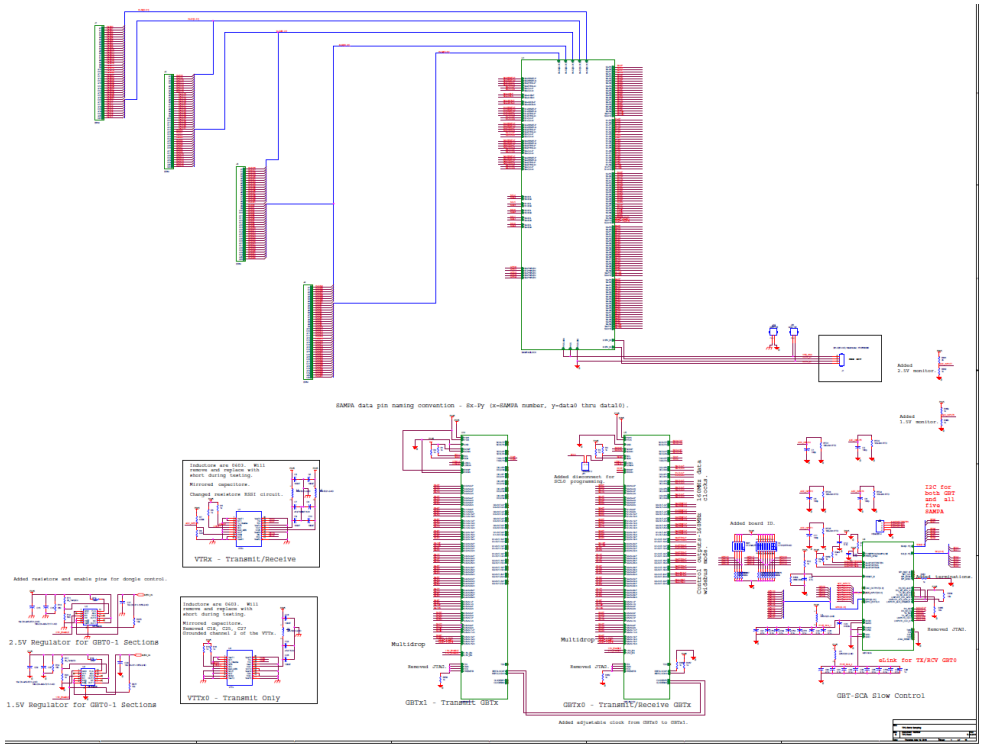


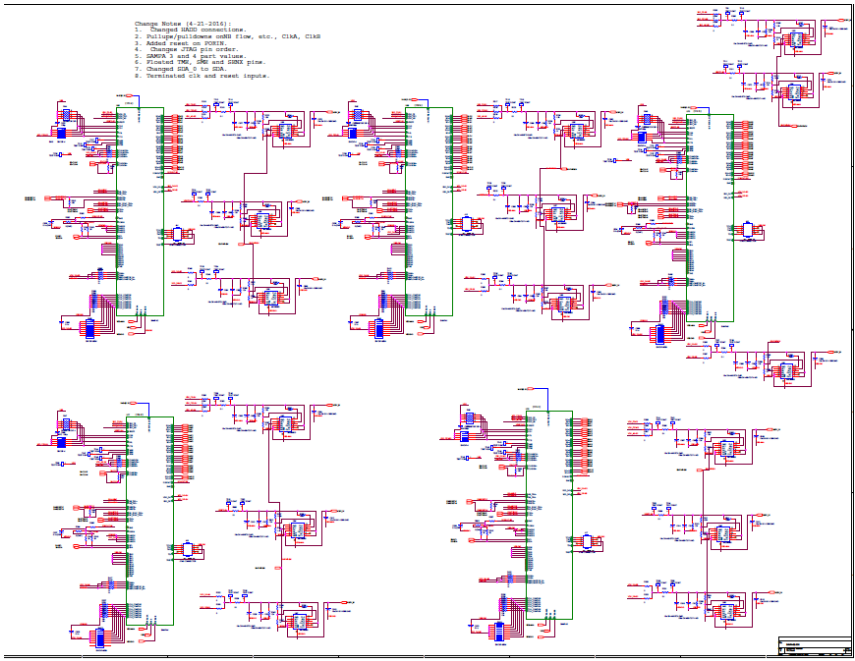
The existing TPC board is our size template



ALICE-USA
BTU Project

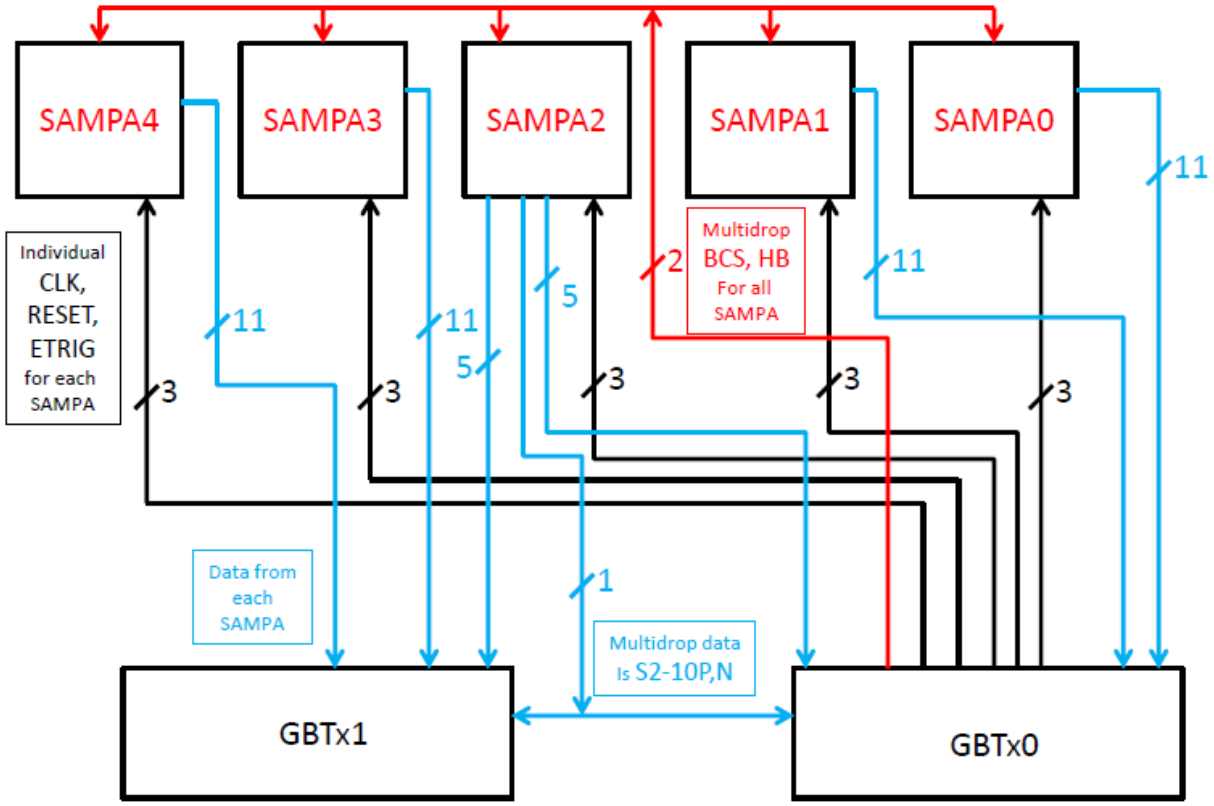
The Beast





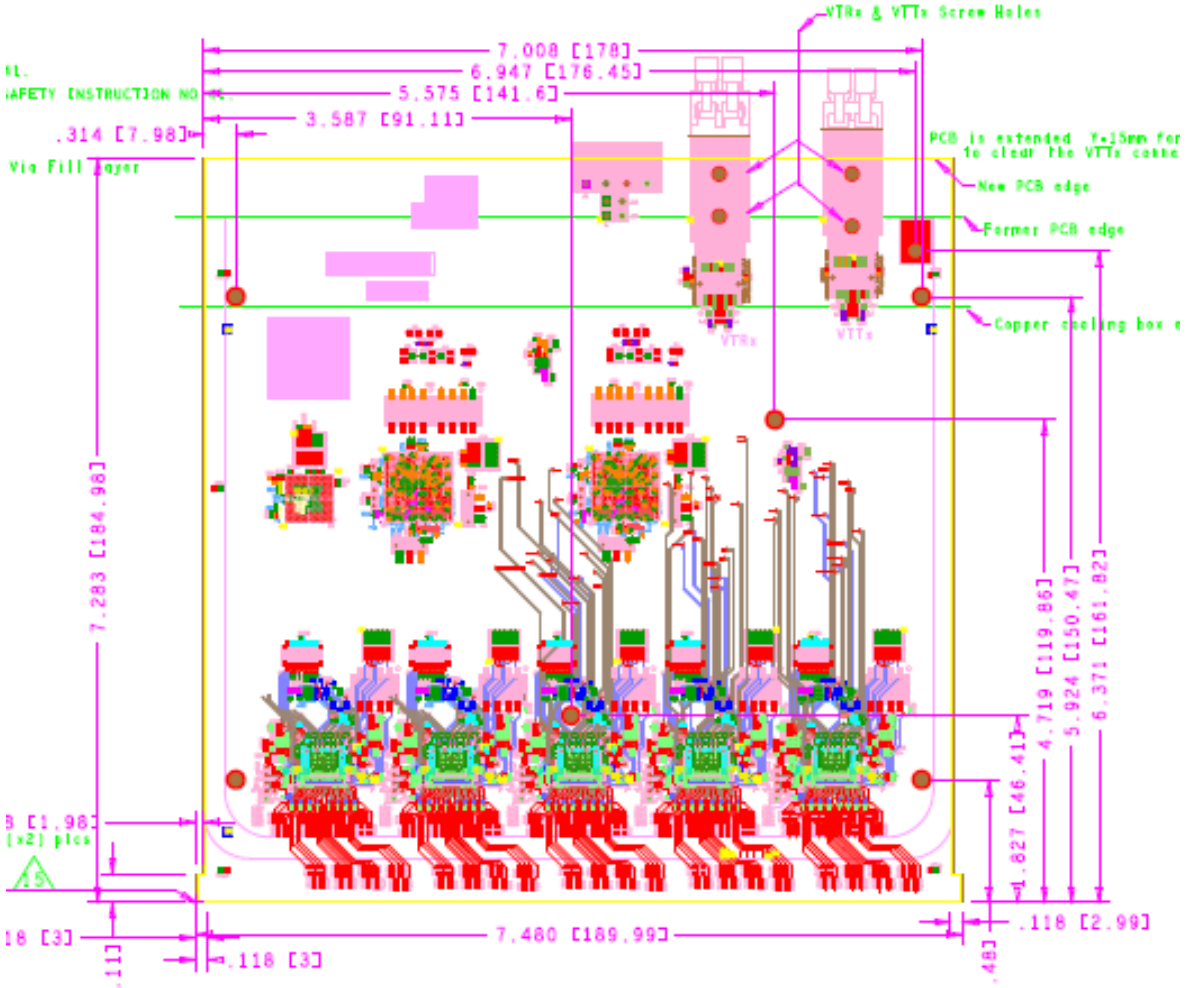
The interconnect block diagram is relatively straightforward

- All clocks, resets, sync, control come from GBTx0
- GBTx1 is only a receiver of data



Board layout is proceeding

- SAMPA layout and connector placement has been the primary focus
- The high-speed line routing is presently under way
- An 8-layer system is our current plan
- Mounting holes and cooling tube is same as current system
- Depth of board will increase by ~0.6”
- Same power connector as current system
- Rev0 will have detachable input cables



Prototyping Stages

- Rev 0 – The initial design
  - Schematic capture
    - Done in Cadence Allegro/Orcad 16.6
    - Design was reviewed prior to layout
  - Layout
    - Danny Simpson, Outside layout engineer used by ORNL.
    - Using Cadence Allegro layout
    - Layout will be reviewed by the collaboration and revised.
    - Rev. 0 rigid-only PCB has these benefits:
      - domestic only (no customs)
      - fastest possible turn-around
      - lowest cost fab for prototyping

Technical approach/challenges

- Rev 0 (cont.)
  - Layout (cont.)
    - We had planned to utilize flexcable for the detector inputs but the cost and turn around was too high
    - We are using detachable cables with ERNI connectors for the detector connection
  - Fabricate
    - We will fabricate up to 20 of the boards
    - 15 will be used for detector test
    - These will be distributed to collaborators for testing
- Rev 1 will repeat the cycle after test results have been received and reviewed
- Rev 1a will be the final pre-production design

ALICE-USA
BTU Project

Technical approach

- CERN requires Halogen-Free material for the boards
- Our regular assembly house can supply this

isola

GreenSpeed™ Halogen Free Laminates and Prepregs

GreenSpeed™ is a halogen free base material that meets the requirements of traditional FR-4 materials. The resin matrix is based on a modified epoxy resin. Conventional E-glass-fabric is used for reinforcement. The requirements of flammability class V-0 as per UL-94 are met without addition of antimony compounds. Since this grade does not contain halogens, it displays greater thermal stability than standard FR-4 materials.

www.isola-group.com/products/GreenSpeed

ORDERING INFORMATION:

Contact your local sales representative or visit **www.isola-group.com** for further information.

Isola Group
3100 West Ray Road
Suite 301
Chandler, AZ 85226
Phone: 480-893-6527
Fax: 480-893-1409
info@isola-group.com

Isola Asia Pacific (Hong Kong) Ltd.
Unit 3512 - 3522, 35/F
No. 1 Hung To Road, Kwun Tong,
Kowloon, Hong Kong
Phone: 852-2418-1318
Fax: 852-2418-1533
info.hkg@isola-group.com

Isola GmbH
Isolastrasse 2
D-52348 Düren, Germany
Phone: 49-2421-8080
Fax: 49-2421-808164
info-dur@isola-group.com

Halogen Free

GreenSpeed™
Data Sheet

Tg 180, Td 395
Dk 4.16, Df 0.0154
/94 /122 /125 /127 /128

Features

- Thermal Performance
  - Tg: 180°C (DSC)
  - Td: 395°C (TGA @ 5% wt loss)
  - Superior performance through multiple thermal excursions
  - Superior chemical and thermal resistance
  - Lower CTE from ambient to 288°C
- T260: >60 minutes
- T288: >60 minutes
- RoHS Compliant
- UV Blocking and AOI Compatible
  - UV blocking and enhanced florescence
  - Compatible with all AOI equipment, including laser-enhanced reflectance systems
- Core Material Standard Availability
  - Thickness: 0.002" (0.05 mm) to 0.093" (2.4 mm)
  - Available in full size sheet or panel form
- Prepreg Standard Availability
  - Roll or panel form
  - Tooling of prepreg panels available
- Copper Foil Type Availability
  - Standard HTE Grade 3
  - RTF (Reverse Treat Foil)
- Copper Weights
  - ½, 1 and 2 oz (18, 38 and 70 µm) available
  - Heavier copper available upon request
  - Thinner copper foil available upon request
- Glass Fabric Availability
  - Standard E-glass
  - Square weave glass fabric available
  - Spread glass fabric available
- Industry Approvals
  - IPC-4101C /94 /122 /125 /127 /128
  - UL - File Number E41625

Production Plan & QA/QC (consistent with testing requirements and acceptance)

- Acceptance tests outlined in **ALICE Barrel Tracking Upgrade Project Management Plan** (Document BTU.1.v4)
- Test stands using CRU will be developed
- Vendor evaluation has started
- Five runs will be used to accomplish the production

ALICE-USA
BTU Project

Hazard Analysis & Mitigation

- BTU.9 Hazard Analysis Document:
  - Describes potential hazards and mitigation for TPC FEC
  - Sealed low voltage power supplies
  - Soldering, lead solder
  - Workers have taken required safety training (electrical safety, chemical safety, PPE).
  - Example: FEC lab posting →
- BTU.8 ES&H Management Plan
  - Follows ORNL ES&H policies
  - Periodic on-site safety reviews

NOTICE

AUTHORIZED PERSONNEL ONLY

See Access Requirements for Details

Space Function	BLDG/RM
Laboratory 1, Dry	6000/211

HAZARD WARNINGS

Access Requirements

Unescorted access to Building 6000 is granted upon completion of facility specific access training.

Obey Radiological Postings.

PPE required for work with chemicals, power tools, soldering, or performing work on or near electrical work.

Research Support Group Leader Charlie Havener, 574-4704, Bldg 6000 Room 250A and Division Director David Dean 576-5229

CONTACTS	NAME	PHONE	OFFICE
Space Manager	Kenneth Read Jr	574-5347	6000 Room 219
Space Group Leader	Thomas Cormier	574-9998	6000 Room 213
Complex Facility Manager	Richard Griffey	574-8907	5700 Room J103
Facility Operations Manager	B Tatum	574-4759	6000 Room 203

LAST REVISION: 9/2/2015 (1)

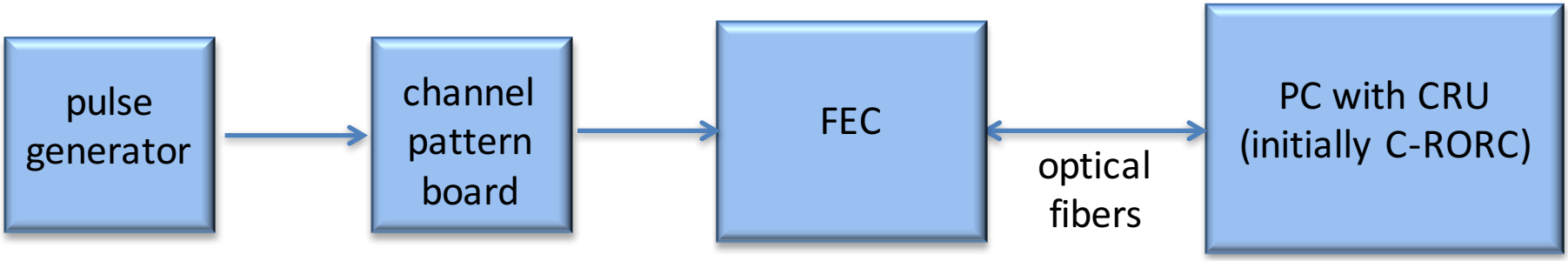
Summary

- MPW1 testing revealed many issues
- Test-campaign deficiencies for MPW1 have been well addressed
- MPW2 appears to have been well simulated (but not complete chip)
- The Rev0 FEC has presented several challenges, primarily cost

Backup slides

ALICE-USA
BTU Project

FEC Test Station



- Testing criteria summarized in Appendix A.2 of BTU.1.v8.
- Can pulse different selected patterns of input channels.
- Will initially use C-RORC FPGA board until CRU becomes available in later 2016.
- FEC test station developed for August 2016 will be improved and used for mass FEC testing in early 2019.

ALICE-USA
BTU Project

FEC Testing Matrix