# TPC DAQ Rate Increase to 5 kHz

## a status report

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# Contents

- TPC rate upgrade to 5 kHz
  - this presentation
- Trigger upgrade to 5 kHz
  - mostly affects EPD QT boards
    - but not in this presentation…
- Other DAQ items (a brief mention)
  - return of BSMD
    - some effort will be needed to reinstall the DAQ side because all the DAQ components have been repurposed
  - FCS new trigger algorithms? TBD

# A reminder from the Feb 2022 Collaboration Meeting:

- redo the FPGA firmware [TL]
  - make sure the VHDL tools are working [done]
  - reformat the data on the fiber to pack it more efficiently (e.g. TPX can gain 30%)
  - setup & support boards in the lab for testing [Christian, Tim]
- redo the DAQ online software [TL]
  - main framework already working for e.g. FCS & STGC – add TPX & iTPC
  - add capability to replay older data for algorithm evaluation
- redo & re-evaluate the cluster finder(s) [TL, Yuri?, others?]
  - rewrite parts of it to make it faster even without changing the algorithm [TL]
  - but also play with algorithms and evaluate them based upon data already taken [TL, Yuri?, ?]
  - play with ZS ASIC cuts to optimize throughput vs tracking efficiency [Yuri?, TL, ?]
- find and download old runs already taken and use the data for: [?]
  - software framework replay and speed evaluation
  - algorithm replay/improvement
  - firmware development [e.g. extract occupancy per FEE which we can feed into the HW, etc]
- better ethernet connectivity [Jeff, Wayne, TL]
- add new DAQ PCs [TL, Wayne, Christian, Tim]
  - refurbish older PCs with more memory [Wayne]
- add new Event Builders [Jeff,...]
- think about modes of running [all]
  - low vs hi lumi?
  - trigger mixes?
  - pre-preliminary Run Control configurations based upon the BUR [Jeff]
- Trigger issues? [all]
  - e.g. can EPD QTs be read out at 5 kHz at all?
- Forward Program impact? [Carl, all]
- Offline computing issues [Jeff, Gene, …]
  - can we store to tape and then analyze this amount of data?
- TPC itself [all]
  - distortions [Gene?]
  - anode currents & other hardware issues? [Alexei?]
- Other TBD [up to the Task Force]

# FPGA Firmware

- Inner TPC (iTPC) 90% completed
  - core firmware is 100% finished on both RDO & FEE FPGAs
    - what still remains are the final touches related to error detection, auto-recovery etc
- Outer TPC (TPX) 70% completed
  - currently working on the full pathway from the FEE to the fiber
    - Mux FPGA 100% completed
    - FEE FPGA 90% completed
    - Main RDO FPGA ~70% completed
- current results for emulated min-bias events
  - 5+ kHz for TPX (but not yet finished)
  - 7+ kHz for iTPC

# Cluster Finder

- faster version of the 2D cluster finder written
  - it is equivalent to the current iTPC cluster finder but performs ~2x faster
    - internal reorganization of memory with additionally optimized data format changes in the hardware FPGAs
- tested on all 3 different DAQ PC types with associated contributions using old data:
  - old TPX PCs (which cover RDOs 3 & 4 of a sector)
  - newer TPX PCs (which cover RDOs 5 & 6 but on 2 sectors)
  - new iTPC PCs (which cover the 4 iTPC RDOs of 1 sector)
- not a bottleneck in the new speedup upgrade
  - e.g. runs at at least 10 kHz for min-bias data
- more testing still needs to be done to iron out potential bugs
  - especially the comparison of the data from the old TPX 1.5D cluster finder with the new 2D flavor
    - since this is now brand new and one can't just do trivial (e.g. bitwise) comparisons

# Other Items from our Feb 2022 list

- new DAQ PCs were not necessary → not purchased
- memory of the very-old TPX PCs successfully upgraded to 8 GB [Wayne]
  - which was required for the new cluster finder
- new Event Builders & revamp of the Event Builder networks [Jeff]
  - in progress

# Conclusion

- all critical pathways of all FPGAs rewritten successfully
  - the “5 kHz” requirement met
    - still needs a bit more work on the TPX side to fix various internal timing issues
  - additional firmware which adds robust handling of errors needs to be added
- rewritten cluster finder performs well
  - speed & memory requirement met on all 3 PC platforms
- I expect to be ready for a full commissioning test by Jan 1st
  - using only noise and artificially created “data” at first
  - but I also expect further tweaks to be added & more debugging as we go especially at the very beginning of the run with real data