Calorimeter (Tile/LAr)
The committee was very impressed by the progress on this technically challenging and important upgrade. The calorimeter team has an experienced, dedicated team of physicists, engineers, and technical staff contributing to project development while ensuring readiness for construction on time and on budget. While especially the calorimeter front end is still in the prototyping stage, all parts do appear to have a credible schedule with potential mitigations built into the schedule where prototyping is present.

1. The project has achieved the necessary level of technical preparation and readiness to begin construction.
    a. 6.4.1 LAr ASICS and optics
        i. Findings: The ASICS are still in the prototyping stage. Several prototypes have been made. The backup ADC chip suffers from SEUs.
        ii. Comment: the extent of the progress on the ASICs is difficult to assess due to inadequate documentation. However, based on the slides provided at the meeting, the progress looks good and seem to be on track for production. The technical presentations had too much on material that was not technical, reducing time available to discuss technical details. For the optics, the lpGBT may be delayed if Run 3 is delayed.
        iii. Recommendation: More words on the slides about various prototyping rounds and their lessons learned would help give confidence that the prototypes are indicative of future success. It should be available before the review. Management should ensure the slides are released to the committee on schedule.
    b. 6.4.2 FEB2
        i. Findings: this project has a large number of external dependencies, on the DOE preamp/shaper and on the optical links. The board also requires a level-0-sum-er child card that has no responsible and might be a US scope increase.
        ii. Comments: While the DOE preamp/shaper is a US project and thus should remain on schedule in the event of a delay for the Run 3 start, the optical links are produced by CERN may be delayed. The addition of the sum-er card to the US scope is an opportunity..
        iii. Recommendations: none
    c. 6.4.3 backend SRTM and firmware
        i. Comments: the interface between the processing fpga and the rest of the sRTM seems well defined so that even if this external fails the project should be able to proceed.
        ii. Recommendations: none
    d. 6.5.4.1,6.5.4.2 LVPS bricks
        i. Findings: this project is a simple extension of a previous successful project. However, the method for using 6 wires to turn on/off 8 bricks is not finalized; there is a recent change in the proposed methodology The

tile community agrees on the change, but it needs to be finalized at cern pdr in september. There is also a vertical slice test is in october. Testing for new method (tri-voltage solution) has been tried on the bricks, but not via the “aux” board off detector in USA16 that feeds into the mother board to the bricks and which is a Prague responsibility.

ii. Comments: Despite the recent change, the project seems on track for production, as the board is relatively straight forward.

iii. Recommendations: none

e. 6.5.2 motherboards

i. Findings: The motherboards have an external dependence on the elmb2 chip. The Elmb2 neutron radiation tests are not complete. Data is not completely analyzed yet. Results from a previous test were marginal, but perhaps due to unknown particle content. Mitigation would be to swap half way through the run.

ii. Comment: since this is important for many CERN applications, the elmb2 will be made to work. The schedule seems to have plenty of time slip. Swapping the power supplies half way through the run should be an acceptable solution.

iii. Recommendations: none

2. Tools and technologies needed to construct the project are available. Industrialization of key technologies needed for construction is complete
   a. LAr ASICS and optics
      i. The most exotic technology needed is for ASIC production. 65 nm and 130 nm technologies are well established
   b. FEB2
   c. backend SRTM and firmware
   d. LVPS bricks
   e. motherboards
3. The project’s scientific and technical contributors are credibly expected to accomplish the proposed work scope within the requested budget and schedule duration.
   a. 6.4.1 LAr ASICS and optics
      i. Findings: Key members of the team working on the LAr ASICS and optics have extensive experience stemming from work on the original ATLAS construction as well as Phase I upgrades.
      ii. Comments: The scope of the technical work being proposed seemed carefully considered and commensurate with the available expertise and the resources requested. It seems very credible that they will accomplish the work within the requested budget and schedule.
      iii. Recommendations: none
   b. 6.4.2 FEB2
      i. Findings: The FEB2 incorporates elements of 6.4.1 and supporting circuitry onto a board to digitize and transmit LAr signals.

ii. Comments: The L3 CAM has extensive and relevant experience dating back to the original ATLAS construction, leading the Columbia group that developed the original FEB and five custom ASICs. The technical progress on the FEB2 is encouraging, with clear steps ahead in remaining R&D and pre-MREFC. The FEB2 estimates are largely in the category of Analogy, but the extensive prior experience with this sort of development lends credibility to this. It seems credible that the work of 6.4.2 will be accomplished within the requested budget and schedule

iii. Recommendations:

c. 6.4.3 backend sRTM and firmware

i. Findings:

ii. Comments: The new "smart" RTM incorporates an FPGA and some of the functionality that had been found on the original FEB, providing LHC clock recovery, synchronization with ATLAS, monitoring functionality, and data transmission to the ATLAS read out system. Members of the team have experience from the design, production, and testing of Phase I ATLAS upgrade LAr trigger board and firmware. Manpower for the firmware development has been increased since the PDR, reflecting experience stemming from Phase I upgrade. It seems credible that the work of 6.4.3 will be accomplished within the requested budget and schedule.

iii. Recommendations:

d. 6.5.4.1, 6.5.4.2 LVPS bricks and 6.5.2 motherboards

i. Findings:

ii. Comments: The team working on these WBS items are very knowledgeable and also specifically experienced with the tilecal electronics. Key members of the team were responsible for the design and implementation of the original tilecal electronics.

iii. Recommendations:

4. The project has finalized all necessary commitments and partnerships, including definition of project deliverables, performing organizations, and schedules.

a. 6.4.1 LAr ASICS and optics-

i. Finding: The ASICs are still in development and hence the schedule is not particularly final at this point. Allowing for changes between the final prototype and the pre-production mitigates the uncertainty to some extent. Overall, the LHC schedule uncertainty as well as the delivery of shared ATLAS/CMS ASICs (lpGBP and the Versitile Link) are large unknowns mostly out of the control of the project.

b. 6.4.2 FEB2

i. Comment: In general, it would be helpful for the review process to match the FEB2 batches to the ATLAS installation schedule visually to highlight the float discussion.

c. 6.5.4.1,6.5.4.2 LVPS bricks
    i. Comment: The discussion on the ELMB2 motherboard cost was confusing and it was not clear to the reviewers what cost will be used in the final schedule. The board cost is supposed to be redone before the NSF FDR.
    ii. Finding: A linkage to a board needed to implement the tri-state solution, but not in control of the NSF project was mentioned, but not obvious from the presentation material.
d. 6.4.3 backend SRTM and firmware
e. 6.5.2 motherboards

5. The project has a defined acquisition strategy for purchased items. Designs, specifications and work scope comprising bid packages to industry are in advanced states of maturity and available for NSF review. Bid packages to be released in FY2020 are sufficiently clear and well defined as to be ready for bid.
    a. 6.4.1 LAr ASICS and optics, 6.4.2 FEB2,6.4.3 backend SRTM and firmware BE, 6.5.4.1,6.5.4.2 LVPS bricks, 6.5.2 motherboards
        i. Finding: For all of these projects except 6.5.2, the current costs of the necessary components has been found. The responsible institution for the purchase has been identified. Bid packages have not yet been developed, as the designs are not yet finalized. For 6.5.2 there are quotes for the manufacture of pc boards in Prague, not in the US
        ii. Comments: The bids should be fairly simple and we don't anticipate problems. But for the tile motherboard, it is not clear the correlation between this price and a price for manufacturing in the U.S..
        iii. Recommendations: US-based price estimates should be obtained for any manufactured item.
6. Performance verification and acceptance test policies for all deliverables are defined and complete. Documentation describes how acceptance tests will verify that deliverables meet design performance specifications and safety requirements.QA plans and activities are integrated into the RLS. QA and radiation exposure policies are applied consistently across the project.
    a. LAr ASICS and optics
        i. Comment: The ATLAS collaboration has internal reviews to establish official specifications and production readiness. This WBS has assurance guidelines from the similar phase 1 project and this should provide a good framework for QA/QC for the deliverables for the production. The collaboration has an irradiation testing policy that subsystems must follow for qualification.
        ii. Comment: We have commented elsewhere that the development prior to production deserves extra scrutiny.
    b. FEB2
        i. See (a: i and ii) above
    c. backend SRTM and firmware

i. See (a: i) above

d. LVPS bricks
   i. See (a: i) above
e. Motherboards
   i. See (a: i) above
   ii. Comment: There were concerns about the long length and via types and complexity of the main board. The project has agreed to consider the whole “bathtub curve” in its testing/burn-in methodology.
   iii. For such a mature design, it should be possible to trace the documentation through all levels. During the drill down to check that a schematic was in EDMS there was some difficulty navigating the documentation chain. The project is aware of this issue and the specific concern was fixed during the review and the project is aware of the general issue now.

7. Project documentation describes how the construction-ready design is derived from the flow-down of science goals to science requirements then on to technical performance specifications and requirements. The documentation is in a format that enables traceability, is clearly explained, and is aggregated into a dedicated section of the PEP.

   There is a dedicated Section 1.2 Science Requirements in the PEP and the summary in section 1.2.1 is a useful compilation of the various science-driven requirements. The path from PEP to TDR is navigable.

   However, there is a recommendation in the January 2018 NSF PDR review report regarding the science flowdown, “Add detailed technical specifications for all systems of the MREFC project to the Science Flowdown document.” and a related comment, “The Science Flowdown document (#269) provides clear logic how high level science requirements are propagated into high level technical specifications, but does not yet extend to sufficiently low for FDR level.” The last listed revision in that document is dated 12/28/2017 so it doesn’t seem to reflect any changes related to the recommendation yet. While the talks on 6.4 and 6.5 did show illustrative examples of science flowdown to technical requirements, the comments from the PDR remain valid.

   a. 6.4.1 LAr ASICS and optics, 6.4.2 FEB2, 6.4.3 backend sRTM and firmware
      i. The talks on these elements did show illustrative examples of science flowdown to specific technical requirements.
   b. 6.5.4.1, 6.5.4.2 LVPS bricks and 6.5.2 motherboards
      i. The requirements on the LVPS bricks and the EMDB motherboards do follow from the science goals of enabling the proper functioning of the tilecal for O(TeV) jet measurements and O(100 MeV) MIP signals in the high rate, high radiation environment of HL-LHC. This importance of the tilecal performance to measurements of physics objects was shown

clearly in the L2 tilecal talk, but see general comment about science flowdown above.

8. All detector functions and requirements are reflected in the Performance Measurement Baseline.
    a. 6.4.1 LAr ASICS and optics
        i. Comment: The ADC ASIC development should be followed closely in the period before the MREFC start. The next iteration, v3, which will be submitted in August is an important step towards the final prototype where multiple ADCs are incorporated in the same package. At this point (of course) it is not known if the multi-ADC chip, v3, will meet goals.
        ii. Finding: The COTS ADC alternative identified as a risk mitigation for the ASIC ADC has a set of risks associated with adoption that make it highly undesirable: e.g. SEU issues.
    b. 6.4.2 FEB2
        i. Comment: The first slice prototype with a multi-ADC ASIC deserves extra scrutiny as it is not known at this point whether a successful multi-ADC ASIC can be incorporated successfully in a multi-chip board.
        ii. Comment: If the v3 ADC ASIC is sufficiently performant, the FEB2 development should be followed closely in the period before the MREFC start.
    c. 6.4.3 backend SRTM and firmware
    d. 6.5.4.1,6.5.4.2 LVPS bricks
    e. 6.5.2 motherboards
9. Specialized technologies enabling the scope fabrication are sufficiently mature to begin construction.
    a. 6.4.1 LAr ASICSand optics
        i. Finding: there are two options for this ASIC. The first choice is a 65 nm technology. A 14 bit ASIC in this technology is still being developed. There is an existing off-the-shelf 14 bit ADC that would be used in case of failure of the 65 nm technology
        ii. Comment: The progress on the 65 nm technology looks good, although the documentation on the performance of the current prototype was inadequate to be sure. Also, the documentation on the tests of the performance on the alternative were not adequate to be sure of its performance, although we were told verbally that they did verify that it had true 14 bit performance. However, due to its Hz rate for SEUs, the backup solution may not be a real backup solution.
        iii. Recommendation: none
    b. 6.4.2 FEB2
    c. 6.4.3 backend SRTM and firmware
    d. 6.5.4.1,6.5.4.2 LVPS bricks
    e. 6.5.2 motherboards

10. Technical scope elements of the performance baseline remain consistent with what was approved for advancement to Final Design stage following PDR.
    a. 6.4.1 LAr ASICS and optics, 6.4.2 FEB2
        i. Findings:
        ii. Comments: The scope presented here seems quite consistent with that presented at PDR
        iii. Recommendations:
    b. 6.4.3 backend sRTM and firmware
        i. Findings:
        ii. Comments: The decision to build the "smart RTM" (sRTM) instead of a "Main Board" and "RTM“ was taken following the PDR. Additional resources for the firmware development have been added to the RLS.
        iii. Recommendations:
    c. 6.5.4.1, 6.5.4.2 LVPS bricks and 6.5.2 motherboards
        i. Findings:
        ii. Comments: The scope presented here seems quite consistent with that presented at PDR
        iii. Recommendations:
11. There is a vetted safety plan and appropriate safety experts are available to the project to implement and oversee the safety plan.
    a. 6.4.1 LAr ASICSand optic
    b. 6.4.2 FEB2
    c. 6.4.3 backend SRTM and firmware
    d. 6.5.4.1,6.5.4.2 LVPS bricks -
        i. Finding: The use of higher voltage (200 V) for the power input seems the most compelling safety issue and the project has taken ownership.
    e. 6.5.2 motherboards
12. Plans and justifications for fabrication of spares within the construction program are defined and well justified.
    a. 6.4.1 LAr ASICS fine
    b. 6.4.2 FEB2 fine
    c. 6.4.3 backend SRTM and firmware
    d. 6.5.4.1,6.5.4.2 LVPS bricks fine
    e. 6.5.2 motherboards fine
13. Plans and schedules for shipment of deliverables to CERN are credible and appropriately integrated into the RLS.

    Comments: The schedules for 6.4 and 6.5 in the RLS seem appropriately detailed, reasonable, and contain explicit milestones for acceptance at CERN. The tilecal schedule has external “need by” milestones in the schedule which is helpful for judging the suitability of schedules leading to that date. Similar explicit “need by” external milestones might be considered for the LAr schedule. The LAr ADC pre-prototype 3 was originally scheduled for May; it is now anticipated for August; if that happens on

schedule and is successful it appears it will allow the schedule for the ATLAS PDR to be maintained.