



# Answers to Sept 11 Questions



- 1. Descope/upscope items - please provide both preferred/scheduled and need-by dates...



# Answers to Sept 11 Questions



- 2. Please provide a schedule of expiration of descope options throughout project. please focus on dates.



# Answers to Sept 11 Questions



- 3. Provide top 5 risks in rank order (worst->least) for each major subsystem.
  - LAr:
    - RN-06-04-02-001 (210) - Delay in launch of FEB2 preproduction
      - Rely on timely delivery of components, incl. PA/S (DOE scope) and lpGBT
    - RN-06-04-01-002 (140) - 65 nm ADC failure (ie. need to adopt COTS ADC)
      - Relatively high rank, despite Low probability, due to high cost impact (\$1.3M)
    - RN-06-04-01-001 (140) - Additional ADC design iteration needed
      - Significant schedule impact, up to 12 mo. – mitigated by baseline of 5 iterations (3 preproto, proto, prod)
    - RN-06-04-01-005 (140) - Additional design iteration needed for optical link components
      - Similar to above, but for lpGBT, VL+
    - RN-06-04-03-004 (140) - LASP and sRTM system density
      - Could have to produce twice as many (lower complexity) sRTM boards



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- 3. Provide top 5 risks in rank order (worst->least) for each major subsystem.
  - Tile:
    - Cost scores for Tile all at 1(Low); Schedule score up to 3(Med)
      - Reasonable responses for all
    - RN-06-05-04-005: (120) delay in receiving LV box parts from collaborator
    - RN-06-05-03-003: (90) ELMBMB production yield lower than expected
    - RN-06-05-01-003: (60) radiation certified MB component no longer avail.
    - RN-06-05-04-001: (60) LV brick redesign due to unavailable component
    - RN-06-05-03-001: (60) ELMB2 potential delays due to CERN board production



# Answers to Sept 11 Questions



- 3. Provide top 5 risks in rank order (worst->least) for each major subsystem.

- Muon:

WBS	Risk-ID	Expected		Title	Summary	Probability Post-Mitig.	Cost Impact (k\$)		Schedule Impact		Risk
		Expiration					Low	High	Low	High	Rank
<b>6.6 Muon Spectrometer (NSF)</b>											
6.6.3 TDC	RN-06-06-03-005	30-Sep-22		loss of ASIC design engineer	The lead ASIC design engineer can not continue to work on the project.	36%	80	120	8.0	12.0	210
6.6.1 sMDT	RN-06-06-01-013	28-Sep-23		Foreign exchange risk for tubes and/or chamber materials.	If the EUR-USD exchange rate becomes significantly less favorable than the assumed rate, the cost of raw materials for tubes and chambers will increase	18%	300	600	-	-	140
6.6.3 TDC	RN-06-06-03-001	10-Jan-22		More than two TDC prototypes are needed before the final production run.	Due to changes of specifications or previous prototypes do not satisfy all requirements, more than two prototype runs are needed.	18%	110	170	6.0	12.0	140
6.6.3 TDC	RN-06-06-03-006	30-Aug-21		Complexity of ASIC testing higher than expected	Testing of the TDC ASIC requires additional engineering and firmware efforts.	18%	50	80	5.0	8.0	140
6.6.5 LOMDT	RN-06-06-05-011	29-Mar-23		Re-design needed	LOMDT design does not meet specifications	18%	250	1,000	5.0	19.0	140



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- 3. Provide top 5 risks in rank order (worst->least) for each major subsystem.
  - Trigger:
    - RN-06-08-02-019: (210) 6.8.2 HTT Architecture Change
    - RN-06-08-02-033: (210) 6.8.2 HTT FPGA resources insufficient
    - RN-06-08-03-008: (210) 6.8.3 Global Loss of key personnel in firmware effort
    - RN-06-08-01-001: (140) 6.8.1 L0Calo Active Splitting Needed
    - RN-06-08-02-030: (140) 6.8.3 HTT Cooling





# Answers to Sept 11 Questions



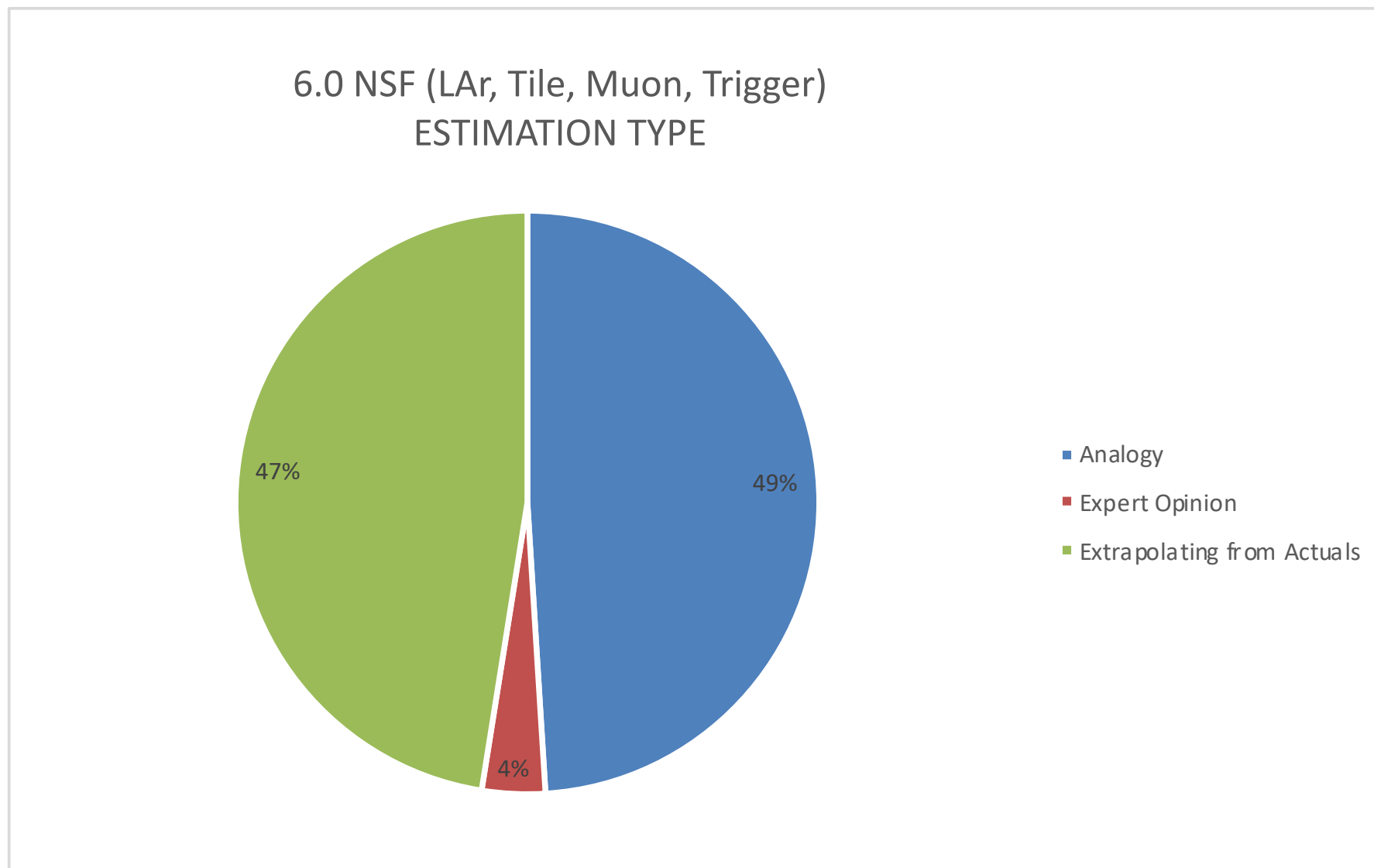
- 4. Please provide a rank-ordered list of remaining work packages (in the pre-MREFC project) - what are you most concerned about? Please mention your “plan B’s”.
  - Muon sMDT chamber-0 construction must be done for site certification, needed to launch production
    - Currently behind schedule, but hoping to catch up before April
    - 257 days of float at this time
  - HTT demonstrator
    - Demonstrator to be fabricated this Fall, but not in hand yet
      - FPGA more complex to implement than those previously used at institutes
    - But boards with ARRIA10 FPGA + 2x48 high speed links ( $\mu$ Pods) are in production (Phase-1 LAr)
      - Technical proof of feasibility in hand



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- 5. Please provide the total project BOE distribution - pie chart format.







# Answers to Sept 11 Questions



- 6. Columbia mgt decision to implement 30 subawards generates a cost impact ~\$186k ... was this to support EV reporting? What did the project gain from this change?
  - This is to further increase robustness of accounting: for example, Chicago is committed to three deliverables:
    - Tile Main Board
    - Trigger HTT (TFM)
    - Trigger Global Algorithm (Hadronic Event Reconstruction)
  - With one sub award, we would have received one monthly invoice from Chicago, with three, we will get one invoice per deliverable
  - Distinct deliverable subawards automatically enforces cleaner financial separation at the institutions as well
  - Well worth the upfront cost



# Answers to Sept 11 Questions



- 7. What risks are being carried forward by the project by the (aggressive?) scheduled downselect of the ADC in December? e.g. radiation tolerance of the ADC ASIC version 3? Please clarify statement on radiation tolerance of commercial ADC option.
  - Schedule is tight, but (based on v2 testing) achievable, with ATLAS PDR (including final approval of decision) in Feb. 2020
  - Getting v3 radiation test completed before MREFC is also tight, though radiation results from v1 and v2 give confidence that the results could be good
    - If radn test comes a bit late, could already start in parallel the first MREFC task, namely (small) design modifications to be made to Prototype based on v3 performance results
  - The COTS ADC was shown by BNL (see JINST 10 (2015) 8009 and p. 25 of J. Parsons' L3 talk for more details) to survive HL-LHC radiation levels. However, in case the COTS solution is chosen, we would want to do some more radiation testing to understand in more detail how to best handle the system impact of the SEU (and particularly) SEFI events



# Answers to Sept 11 Questions



- 8. What is the schedule risk of the late delivery of the production version of IpGBT?
  - See Q12



# Answers to Sept 11 Questions



- 9. Please restate/clarify Scientific travel – where is it covered in the MREFC award? Suggest: please produce List of significant things not in there yet.... don't let us find them.
  - To our knowledge, nothing is missing from the RLS
  - We are evaluating supporting funding for travel for L2s and CAMs for the annual NSF reviews
    - Segregation of funding makes that very complex
      - (See IG examples from last Large Facilities Workshop)
    - If we find a good solution, will implement via BCP



# Answers to Sept 11 Questions



- 10. For each subsystem - what are the (5) major technical requirements, and what is your assessment of your ability to meet them (and what is the basis of that assessment?). Please trace one major science/technical specification from the international ATLAS specification, through your US ATLAS specification set, indicate where addressed in design, and demonstrate how you intend to assess compliance.



# Answers to Sept 11 Questions



- **6.4.1 FE Electronics**
  - **ADC – 40 MSPS, > 11-bit ENOB, 14-bit dynamic range**
    - Achieved in v2, with further improvements implemented in v3 to try gain some additional margin
    - Measured in standalone ASIC tests, as well as on FEB2 (pre)prototypes
  - **lpGBT – 10 Gbps, < 5 ps jitter**
    - Achieved in first prototype, design being iterated to improve radn tolerance
    - Measured in standalone ASIC tests, as well as on FEB2 (pre)prototypes
- **6.4.2 FEB2**
  - **16-bit dynamic range, < 5% coherent noise**
    - To be measured on FEB2 (pre)prototypes (with promising prelim. results already from Analog Testboard), and finally FE Crate System Test
- **6.4.3 BE Electronics**
  - **High-speed (up to 25 Gbps) interconnects LASP-sRTM and sRTM-FELIX**
    - To be measured on sRTM+test card, and finally in BE Crate System Test





# Answers to Sept 11 Questions



- 5 major Tile specs:
  - 6.5.1 Main Board (iATLAS spec doc in EDMS)
    - Serialize data at 560 MHz
    - Digitize with noise  $\leq 3$  ADC counts
    - Radiation tolerance to ATLAS simulations
  - 6.5.3 and 6.5.4 LVPS (iATLAS spec doc in EDMS)
    - Provide +10V (acceptable range 8-16 v) to main Board
    - Radiation tolerance to ATLAS simulations
- Compliance:
  - 6.5.1:
    - all functionality demonstrated in prototype tests
    - Radiation certification for all components expect 2 replacements (retesting now)
  - 6.5.3,6.5.4:
    - All functionality demonstrated in prototype tests
    - Radiation re-testing in progress on replacement components



# Answers to Sept 11 Questions



- Muon

WBS	Specification	Defined Where	Assessment	Basis
6.6.1 (sMDT)	Wire location precision of 20 $\mu$ m	ATLAS FDR and PRR sMDT Tubes Report <a href="https://edms.cern.ch/document/2048104/1">https://edms.cern.ch/document/2048104/1</a>  PDR for sMDT Chambers <a href="https://edms.cern.ch/document/2145116/1">https://edms.cern.ch/document/2145116/1</a>	Already achieved.	-
6.6.3 (TDC)	Power Consumption < 360 mW	ATLAS Technical Specs Document <a href="https://edms.cern.ch/document/1974227/1">https://edms.cern.ch/document/1974227/1</a>	Already achieved.	-
6.6.3 (TDC)	Fine time uniformity <100ps	ATLAS Technical Specs Document <a href="https://edms.cern.ch/document/1974227/1">https://edms.cern.ch/document/1974227/1</a>	Already achieved.	-
6.6.4 (CSM)	Lifetime radiation tolerance	ATLAS Technical Specs Document <a href="https://edms.cern.ch/document/2215051/1">https://edms.cern.ch/document/2215051/1</a>	Achievable	50 krad estimated with safety factors. All components already meet this specification.
6.6.5 (LOMDT)	L0 Latency of 10 $\mu$ s	ATLAS Technical Specs Document (in progress) <a href="https://cds.cern.ch/record/2681225">https://cds.cern.ch/record/2681225</a>	Achievable	Engineering estimate, now being confirmed in FW simulation.



# Answers to Sept 11 Questions



- Trigger

- L0Calo

- Optical light transmission from the tile calorimeter TDAQi optical links must be transmitted to the FEX processors with a maximum -6 dB light intensity loss.
  - Compliance: based on successful Phase-1 system

- HTT

- TP+RTM links speeds operate at 10 Gbps (30 RTM links, 2x13 backplane links, and 32 mezzanine links)
  - Compliance: similar boards have been built, designs are advanced with no show stoppers seen yet
- TFM provides 290 fits per events at 100 kHz
  - Compliance: extrapolation from existing FTK firmware

- Global

- Framework schedules and simultaneously processes algorithms using 5% or less of the resources available on the FPGA
  - Compliance: engineering estimate
- Clustering algorithm uses less than 10% of FPGA resources and has a latency of less than 2000 ns
  - Compliance: test firmware has been implemented with many of the required features, resource usage and latency are well within the bounds



# Answers to Sept 11 Questions



- 11. Please describe the connections between the EPO manager, the L2 managers, and the EPO proponents at the partner universities. How is communication/coordination occurring between these groups? How specifically will the project take advantage of community initiatives like QUARKNET? Give examples of joint activities being considered.



# Answers to Sept 11 Questions



- 12. How exposed is the US project to CERN Project Management uncertainties in schedule? If CERN schedule drifts across many subsystems, could the US project be negatively impacted beyond current expectations?
  - Two cases:
    - Schedule shifts in deliverables US project depends on
    - Overall CERN schedule shift





# External Dependencies



- The L3 talks have slide(s) on external dependencies where they exist, quick summary:

WBS		Collaborator components	Comments				
6.4.1	FE Electronics						
6.4.2	FEB2	IpGBT, VL+	Prod start 1/2023, 40k/all IpGBT available end 2021/mid-2022				
6.4.3	BE Electronics						
6.5.1	Main Board						
6.5.3	ELMB MB	ELMB2 spec	Available				
6.5.4	LVPS						
6.6.1	sMDT						
6.6.3	TDC						
6.6.4	CSM	IpGBT, VL+, GBT-SCA, (FEAST)	Prod start 1/2021, CSM has 390 days of float				
6.6.5	LOMDT						
6.8.1	LOCalo						
6.8.2	HTT						
6.8.3	Global Event Processor						

- Current devices are good enough for all development work, so would only impact production
- IpGBT is latest to arrive, unlikely to impact FEB2 (but see risk RN-06-04-02-001); likely to impact CSM (see risk RN-06-06-04-003)
  - First CSMs needed in early 2024, so sufficient float available





# Overall Schedule Shift



- This Fall, meetings to discuss need for shift in LS3
  - All indications are LS3 may be delayed by one year (schedules very tight for some ATLAS and CMS deliverables, significant risk realized for accelerator)
  - Decision should be announced November 27
  - If LS3 is delayed, float increases by one year
    - It is our intention to move forward as planned, staying with our baseline
    - However, we are all human, and float increase will affect our approach
  - To address this, have added a “CERN delay” risk



# Overall Schedule Shift



- CERN delay risk?
  - To estimate the impact of a CERN delay risk, can look at Phase-I, as LS2 was delayed by 6 months **after** we baselined
    - Both NSF and DOE Phase-I projects were governed by DOE 413.3b
  - In LAr in Phase-I, we used up all the CD-2 schedule contingency + the added amount from the LS2 delay
    - Available time influences decisions on how to address features found during integration
    - However, while we used up ~18 months of schedule float (in a 4 year project), we only used 9% contingency, of which 0 went to “standing army” costs, but maybe 2% can be assigned to extra checks we would not have done if the extra 6 months had not been available
  - In TDAQ in Phase-I, similar situation
    - Of ~25% contingency drawn, none to “standing army” but maybe ~2-7% can be linked to extra time available
- We have added a risk with cost impact 2-7% of \$55M base cost, moderate probability (i.e. 63% in simulation), now our biggest risk