Question 1

- Descope/upscope items - please provide both preferred/scheduled and need-by dates...

SCOPE OPPORTUNITY					
Priority	**System**	**Description**	**Early Decision**	**Latest Decision**	**Cost k$**
1	6.04 LAr	Design and produce Layer Sum Boards (LSB) to be installed on FEB2 boards to implemement HL-LHC Level 0 trigger	Apr-20	Jan-22	700
2	6.05 Tile	Produce additional 50% of LV bricks	Apr-21	Jul-22	540
3	6.05 Tile	Produce additional 50% of LV boxes	Jul-21	Oct-22	325
4	6.08 Trigger	Participate in L1Track	Jan-24	---	2,000
5	6.06 Muon	Purchase remaining L0MDT ATCA crate	May-24	---	34
6	6.04 LAr	Expand US responsibility for firmware for BE electronics (LASP + sRTM)	Apr-20	Jan-23	1,000
7	6.08 Trigger	Additional Global Algorithm	Oct-22	Jan-24	600
8	6.08 Trigger	New Algorithm for L0Calo gFEX	Oct-22	Jan-24	600
9	6.06 Muon	Firmware for NSW Trigger Processor	Oct-21	Oct-23	500
		TOTAL SCOPE OPPORTUNITY			**6,299**

- Some of these (eg LAr BE firmware) could be done partially, at the cost of smaller impact
  - Also smaller impact if decision comes later

Questions 1 and 2

- Please provide a schedule of expiration of descope options throughout project. please focus on dates.
  - These are the expiration dates
  - Note that we already broke down sMDT in 4 blocks

SCOPE CONTINGENCY				
Priority	**System**	**Description**	**Decision**	**Cost Savings (k$)**
1	6.08 Trigger	Reduce HTT capacity 1: make 70% of planned TP, 31% of planned RTM boards, and 83% of planned TFM boards	Jul-23	1,708
2	6.08 Trigger	Reduce HTT capacity 2: further reduce production to 40% of planned TP, 0 RTM boards, and 67% of planned TFM boards	Jul-23	1,619
3	6.06 Muon	Reduce number of sMDT chambers. Do not make chamber sets 5	Dec-21	580
4	6.06 Muon	Reduce number of sMDT chambers. Do not make chamber sets 6	May-22	583
5	6.06 Muon	Do not build L0MDT Command Module in US	Jun-23	594
6	6.06 Muon	Reduce number of sMDT chambers. Do not make chamber sets 7	Sep-22	592
7	6.06 Muon	Reduce number of sMDT chambers. Do not make chamber sets 8	Jan-23	590
8	6.06 Muon	Do not build L0MDT. MDT data to be read out by Felix via another hardware board	Mar-23	810
9	6.04 LAr	Read only 1 gain from FE to BE instead of both HI/LO gain - as a result, build only 50% of sRTM BE boards	Sep-23	1,297
		TOTAL SCOPE CONTINGENCY		**8,373**

Question 3

- Provide top 5 risks in rank order (worst->least) for each major subsystem.
  - LAr:
    - RN-06-04-02-001 (210) - Delay in launch of FEB2 preproduction
      - Rely on timely delivery of components, incl. PA/S (DOE scope) and lpGBT
    - RN-06-04-01-002 (140) - 65 nm ADC failure (ie. need to adopt COTS ADC)
      - Relatively high rank, despite Low probability, due to high cost impact ($1.3M)
    - RN-06-04-01-001 (140) - Additional ADC design iteration needed
      - Significant schedule impact, up to 12 mo. – mitigated by baseline of 5 iterations (3 preproto, proto, prod)
    - RN-06-04-01-005 (140) - Additional design iteration needed for optical link components
      - Similar to above, but for lpGBT, VL+
    - RN-06-04-03-004 (140) - LASP and sRTM system density
      - Could have to produce twice as many (lower complexity) sRTM boards

Question 3

- Provide top 5 risks in rank order (worst->least) for each major subsystem.
  - Tile:
    - Cost scores for Tile all at 1(Low); Schedule score up to 3(Med)
      - Reasonable risk responses for all
    - RN-06-05-04-005: (120) delay in receiving LV box parts from collaborator
    - RN-06-05-03-003: (90) ELMBMB production yield lower than expected
    - RN-06-05-01-003: (60) radiation certified MB component no longer avail.
    - RN-06-05-04-001: (60) LV brick redesign due to unavailable component
    - RN-06-05-03-001: (60) ELMB2 potential delays due to CERN board production

Question 3

- Provide top 5 risks in rank order (worst->least) for each major subsystem.
  - Muon:

		Expected			Probability	Cost Impact (k$)		Schedule Impact		Risk
WBS	Risk-ID	Expiration	Title	Summary	Post-Mitig.	Low	High	Low	High	Rank
6.6 Muon Spectrometer (NSF)										
6.6.3 TDC	RN-06-06-03-005	30-Sep-22	loss of ASIC design engineer	The lead ASIC design engineer can not continue to work on the project.	36%	80	120	8.0	12.0	210
6.6.1 sMDT	RN-06-06-01-013	28-Sep-23	Foreign exchange risk for tubes and/or chamber materials.	If the EUR-USD exchange rate becomes significantly less favorable than the assumed rate, the cost of raw materials for tubes and chambers will increase	18%	300	600	-	-	140
6.6.3 TDC	RN-06-06-03-001	10-Jan-22	More than two TDC prototypes are needed before the final production run.	Due to changes of specifications or previous prototypes do not satisfy all requirements, more than two prototype runs are needed.	18%	110	170	6.0	12.0	140
6.6.3 TDC	RN-06-06-03-006	30-Aug-21	Complexity of ASIC testing higher than expected	Testing of the TDC ASIC requires additional engineering and firmware efforts.	18%	50	80	5.0	8.0	140
6.6.5 L0MDT	RN-06-06-05-011	29-Mar-23	Re-design needed	L0MDT design does not meet specifications	18%	250	1,000	5.0	19.0	140

Question 3

- Provide top 5 risks in rank order (worst->least) for each major subsystem.
  - Trigger:

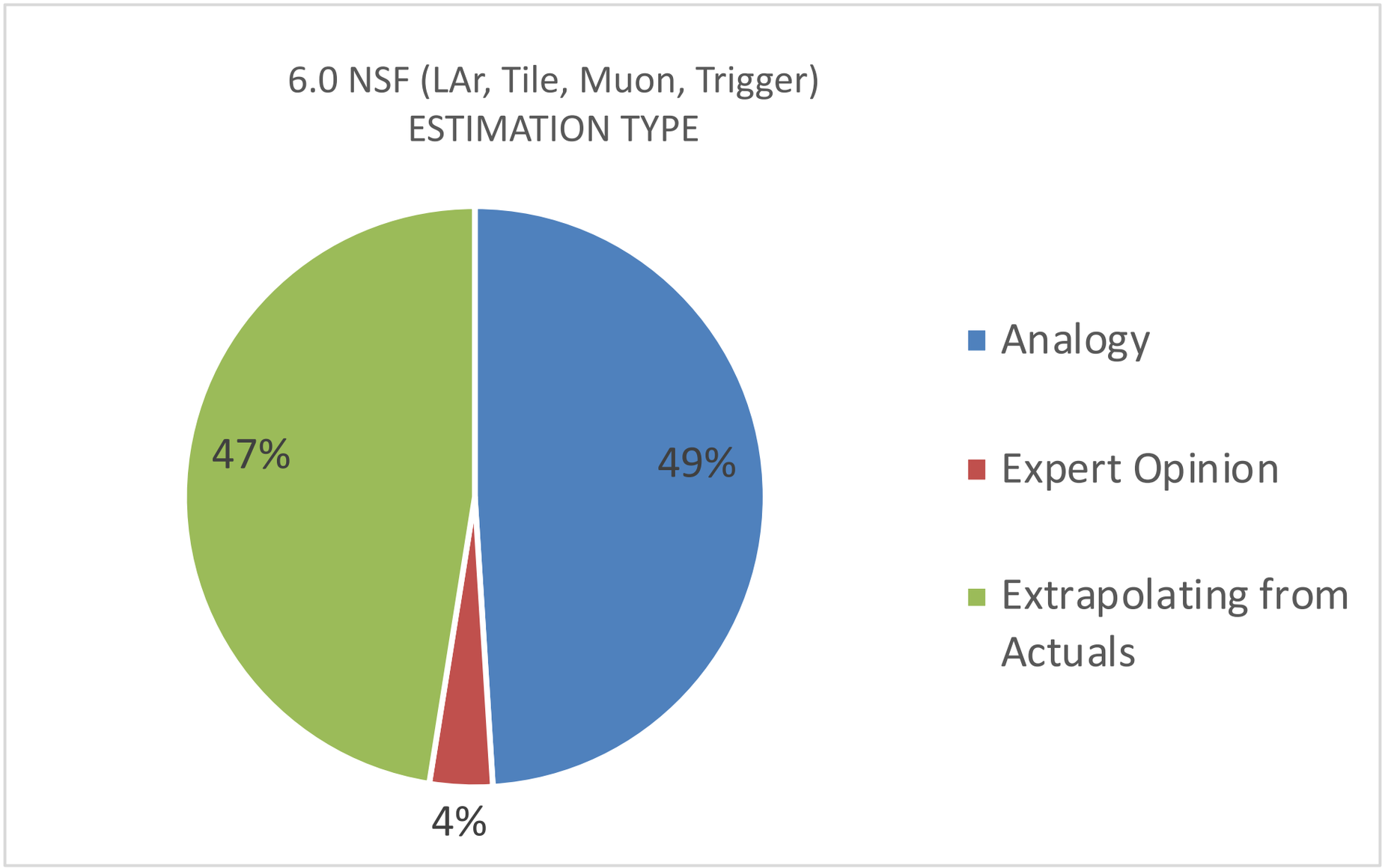
- RN-06-08-02-019: (210) 6.8.2 HTT Architecture Change
  - The system architecture is determined not do statisfy goals or external requirements modified leading to a change in the specifications or number of boards needed. E.g. power consumption is too high and more boards are needed to distribute the power load over more crates.
- RN-06-08-02-033: (210) 6.8.2 HTT FPGA resources insufficient
  - FPGA resource needs are larger than BoE design and the boards need to be designed with a larger FPGA
- RN-06-08-03-008: (210) 6.8.3 Global Loss of key personnel in firmware effort
  - A firmware engineer/technician leaves the project and a replacement needs to be found for work to continue.
- RN-06-08-01-001: (140) 6.8.1 L0Calo Active Splitting Needed
  - Required cable mapping needs 1 to 4 splittings, then an active splitter maybe needed. This would require additional engineering work to develop.
- RN-06-08-02-030: (140) 6.8.3 HTT Cooling
  - TP configuration uses too much power to be cooled effectively or the heat sinks cannot be configured effectively to cool FPGAs

Question 4

- 4. Please provide a rank-ordered list of remaining work packages (in the pre-MREFC project) - what are you most concerned about? Please mention your “plan B’s”.
  - Muon sMDT chamber-0 construction must be done for site certification, needed to launch production
    - Currently behind schedule, but hoping to catch up before April
    - Plan B is eat float; 257 days of float at this time
  - HTT demonstrator
    - Demonstrator to be fabricated this Fall, but not in hand yet
      - FPGA more complex to implement than those previously used at institutes
    - But boards with ARRIA10 FPGA + 2x48 high speed links (µpods) are in production (Phase-1 LAr)
      - Technical proof of feasibility in hand
    - Plan B is eat float

Question 5

- 5. Please provide the total project BOE distribution - pie chart format.



Question 6

- 6. Columbia mgt decision to implement 30 subawards generates a cost impact ~$186k ... was this to support EV reporting? What did the project gain from this change?
  - This is to further increase robustness of accounting: for example, Chicago is committed to three deliverables:
    - Tile Main Board
    - Trigger HTT (TFM)
    - Trigger Global Algorithm (Hadronic Event Reconstruction)
  - With one sub award, we would have received one monthly invoice from Chicago, with three, we will get one invoice per deliverable
  - Distinct deliverable subawards automatically enforces cleaner financial separation at the institutions as well
  - Well worth the upfront cost

Question 7

- 7. What risks are being carried forward by the project by the (aggressive?) scheduled downselect of the ADC in December? e.g. radiation tolerance of the ADC ASIC version 3? Please clarify statement on radiation tolerance of commercial ADC option.
  - Schedule is tight, but (based on v2 testing) achievable, with ATLAS PDR (including final approval of decision) in Feb. 2020
    - Prototype submission in Sept 2020 very much achievable
  - Getting v3 radiation test completed before MREFC is tight, though radiation results from v1 and v2 give confidence that the results will be good
    - If radn test comes a bit late, can start MREFC work, namely (small) design modifications to be made to Prototype based on v3 performance results
  - The COTS ADC was shown by BNL (see JINST 10 (2015) 8009 and p. 25 of J. Parsons' L3 talk for more details) to survive HL-LHC radiation levels. However, in case the COTS solution is chosen, we would want to do some more radiation testing to understand in more detail how to best handle the system impact of the SEU (and particularly) SEFI events

Question 8

- 8. What is the schedule risk of the late delivery of the production version of lpGBT?

WBS		Collaborator components	Comments
6.4.1	FE Electronics		
6.4.2	FEB2	lpGBT, VL+	Prod start 1/2023, 40k/all lpGBT available end 2021/mid-2022
6.4.3	BE Electronics		
6.5.1	Main Board		
6.5.3	ELMB MB	ELMB2 spec	Available
6.5.4	LVPS		
6.6.1	sMDT		
6.6.3	TDC		
6.6.4	CSM	lpGBT, VL+, GBT-SCA, (FEAST)	Prod start 1/2021, CSM has 390 days of float
6.6.5	L0MDT		
6.8.1	L0Calo		
6.8.2	HTT		
6.8.3	Global Event Processor		

- Current lpGBT fine for design/prototype work
- Only CSM production likely to be affected
  - CSM has 390 working days of float

Question 9

- 9. Please restate/clarify Scientific travel – where is it covered in the MREFC award? Suggest: please produce List of significant things not in there yet.... don't let us find them.
  - To our knowledge, nothing is missing from the RLS
  - We are evaluating supporting funding for travel for L2s and CAMs for the annual NSF reviews
    - Segregation of funding makes that very complex
      - (See IG examples from last Large Facilities Workshop)
    - Need to discuss with NSF
    - If we find a good solution, will implement via BCP

Question 10

- 10. For each subsystem - what are the (5) major technical requirements, and what is your assessment of your ability to meet them (and what is the basis of that assessment?). Please trace one major science/technical specification from the international ATLAS specification, through your US ATLAS specification set, indicate where addressed in design, and demonstrate how you intend to assess compliance.

Question 10

- 6.4.1 FE Electronics
  - ADC – 40 MSPS, > 11-bit ENOB, 14-bit dynamic range
    - Achieved in v2, with further improvements implemented in v3 to try gain some additional margin
    - Measured in standalone ASIC tests, as well as on FEB2 (pre)prototypes
  - lpGBT – 10 Gbps, < 5 ps jitter
    - Achieved in first prototype, design being iterated to improve radn tolerance
    - Measured in standalone ASIC tests, as well as on FEB2 (pre)prototypes
- 6.4.2 FEB2
  - 16-bit dynamic range, < 5% coherent noise
    - To be measured on FEB2 (pre)prototypes (with promising prelim. results already from Analog Testboard), and finally FE Crate System Test
- 6.4.3 BE Electronics
  - High-speed (up to 25 Gbps) interconnects LASP-sRTM and sRTM-FELIX
    - To be measured on sRTM+test card, and finally in BE Crate System Test

Question 10

- 5 major Tile specs (also see US spec summary on next slide):
  - 6.5.1 Main Board (iATLAS spec doc in EDMS)
    - Serialize data at 560 MHz
    - Digitize with noise <= 5 ADC counts
    - Radiation tolerance to ATLAS simulations
  - 6.5.3 and 6.5.4 LVPS (iATLAS spec doc in EDMS)
    - Provide +10V (acceptable range 8-16 v) to main Board
    - Radiation tolerance to ATLAS simulations
- Compliance:
  - 6.5.1:
    - all functionality demonstrated in prototype tests
    - Radiation certification for all components expect 2 replacements (retesting now)
  - 6.5.3,6.5.4:
    - All functionality demonstrated in prototype tests
    - Radiation re-testing in progress on replacement components

Question 10

- Muon

WBS	Specification	Defined Where	Assessment	Basis
6.6.1 (sMDT)	Wire location precision of 20µm	ATLAS FDR and PRR sMDT Tubes Report https://edms.cern.ch/document/2048104/1 PDR for sMDT Chambers https://edms.cern.ch/document/2145116/1	Already achieved.	-
6.6.3 (TDC)	Power Consumption < 360 mW	ATLAS Technical Specs Document https://edms.cern.ch/document/1974227/1	Already achieved.	-
6.6.3 (TDC)	Fine time uniformity <100ps	ATLAS Technical Specs Document https://edms.cern.ch/document/1974227/1	Already achieved.	-
6.6.4 (CSM)	Lifetime radiation tolerance	ATLAS Technical Specs Document https://edms.cern.ch/document/2215051/1	Achievable	50 krad estimated with safety factors. All components already meet this specification.
6.6.5 (L0MDT)	L0 Latency of 10µs	ATLAS Technical Specs Document (in progress) https://cds.cern.ch/record/2681225	Achievable	Engineering estimate, now being confirmed in FW simulation.

Question 10

- Trigger

- L0Calo
  - Optical light transmission from the tile calorimeter TDAQi optical links must be transmitted to the FEX processors with a maximum -6 dB light intensity loss.
    - Compliance: based on successful Phase-1 system
- HTT
  - TP+RTM links speeds operate at 10 Gbps (30 RTM links, 2x13 backplane links, and 32 mezzanine links)
    - Compliance: similar boards have been built, designs are advanced with no show stoppers seen yet
  - TFM provides 290 fits per events at 100 kHz
    - Compliance: extrapolation from existing FTK firmware
- Global
  - Framework schedules and simultaneously processes algorithms using 5% or less of the resources available on the FPGA
    - Compliance: engineering estimate
  - Clustering algorithm uses less than 10% of FPGA resources and has a latency of less than 2000 ns
    - Compliance: test firmware has been implemented with many of the required features, resource usage and latency are well within the bounds

Question 11

- Please describe the connections between the EPO manager, the L2 managers, and the EPO proponents at the partner universities. How is communication/coordination occuring between these groups? How specifically will the project take advantage of community initiatives like QUARKNET? Give examples of joint activities being considered.
  - EPO will be considered a part of the reporting by institutions to the L2 managers overseeing their activities. Each institution will consider having a dedicated EPO contact for this, or have their L3 or L4 include EPO as part of their project responsibilities. Each institution will regularly report student numbers, survey data, and participation in the planned project-wide student meetings. The L2 managers will collate this information to report to the HL-LHC EPO coordinator who will coordinate the analysis of the survey data (together with CMS) and keep track of diversity and inclusion goals across the project. To make these links and expectations clear, an additional branch will be added to the US-ATLAS HL-LHC organizational chart

Question 11

- Please describe the connections between the EPO manager, the L2 managers, and the EPO proponents at the partner universities. How is communication/coordination occuring between these groups? How specifically will the project take advantage of community initiatives like QUARKNET? Give examples of joint activities being considered.
  - Initiatives such as Quarknet (and REU) are independent from MREFC EPO, but indeed have resources we can utilize. It is envisioned that the increased US-LHC contributions to Quarknet will provide an opportunity to involve quarknet management in an HL-LHC EPO committee (chaired by the HL-LHC EPO coordinator) charged with formulating meaningful metrics, milestones, outcomes, comparisons, etc..
  - Quarknet trains HS teachers, who then go back to their schools to teach/ train HS students. Although not fleshed out, we could consider using this (or a similar mechanism) to address pipeline diversity by including these HS students in the broader URM networks we plan to establish, and which is a major component to our EPO plan

Question 12

- 12. How exposed is the US project to CERN Project Management uncertainties in schedule? If CERN schedule drifts across many subsystems, could the US project be negatively impacted beyond current expectations?
  - Two cases:
    - Schedule shifts in deliverables US project depends on
    - Overall CERN schedule shift

External Dependencies

- The L3 talks have slide(s) on external dependencies where they exist, quick summary:

WBS		Collaborator components	Comments				
6.4.1	FE Electronics						
6.4.2	FEB2	lpGBT, VL+	Prod start 1/2023, 40k/all lpGBT available end 2021/mid-2022				
6.4.3	BE Electronics						
6.5.1	Main Board						
6.5.3	ELMB MB	ELMB2 spec	Available				
6.5.4	LVPS						
6.6.1	sMDT						
6.6.3	TDC						
6.6.4	CSM	lpGBT, VL+, GBT-SCA, (FEAST)	Prod start 1/2021, CSM has 390 days of float				
6.6.5	L0MDT						
6.8.1	L0Calo						
6.8.2	HTT						
6.8.3	Global Event Processor						

  - Current devices are good enough for all development work, so would only impact production
  - lpGBT is latest to arrive, unlikely to impact FEB2 (but see risk RN-06-04-02-001); likely to impact CSM (see risk RN-06-06-04-003)
    - First CSMs needed in early 2024, so sufficient float available

Overall Schedule Shift

- This Fall, meetings to discuss need for shift in LS3
  - All indications are LS3 may be delayed by one year (schedules very tight for some ATLAS and CMS deliverables, significant risk realized for accelerator)
  - Decision should be announced November 27
  - If LS3 is delayed, float increases by one year
    - It is our intention to move forward as planned, staying with our baseline
    - However, we are all human, and float increase will affect our approach
  - To address this, have added a “CERN delay” risk

Overall Schedule Shift

- CERN delay risk?
  - To estimate the impact of a CERN delay risk, can look at Phase-I, as LS2 was delayed by 6 months **after** we baselined
    - Both NSF and DOE Phase-I projects were governed by DOE 413.3b
  - In LAr in Phase-I, we used up all the CD-2 schedule contingency + the added amount from the LS2 delay
    - Available time influences decisions on how to address features found during integration
    - However, while we used up ~18 months of schedule float (in a 4 year project), we only used 9% contingency, of which 0 went to "standing army" costs, but maybe 2% can be assigned to extra checks we would not have done if the extra 6 months had not been available
  - In TDAQ in Phase-I, similar situation
    - Of ~25% contingency drawn, none to "standing army" but maybe ~2-7% can be linked to extra time available
- We have added a risk with cost impact 2-7% of $55M base cost, moderate probability (i.e. 63% in simulation), now our biggest risk