

Addendum to COVID BCP NSF-1045

March 2, 2022

The NSF COVID BCP (NSF-1045) was developed following the NSF guidance on handling COVID impacts, and follows earlier NSF COVID BCPs (NSF-1033 and NSF-1038). This BCP addresses the impact on schedules and costs due to COVID-19 impacts for the period 5/1/21-3/1/22. Specifically, the following guidance for updating the RLS was provided to the US ATLAS L2 managers and their teams.

- **Completed Tasks**: those tasks (through 3/1/22) remained unchanged. Note that any COVID-19 cost impacts for those tasks, mainly due to inefficiencies, have been tracked separately but are not part of this BCP.
- **In-Progress Tasks**: tasks that were in progress on 3/1/22 were split into two separate tasks. The first task is treated as a completed task and remains unchanged. The second task starts on 3/1/22 and the durations and resources were adjusted by the CAMs taking into account the COVID-19 impacts (*e.g.* COVID-19 delays due to inefficiencies, lab COVID-19 safety requirements, COVID-19 supply chain and vendor delays, etc).
- **Non-Started Tasks**: tasks that were scheduled to start during the period 5/1/21-3/1/22, but in fact did not because of COVID-19 delays, were moved to start after 3/1/22 with the resources unchanged (note that costs may change because of escalation effects).
- **Near-Term Tasks**: if some near-term tasks (at most a few months in the future) have known impacts from COVID-19, they could be adjusted.
- **Travel**: tasks that are for travel that is known to be cancelled, *e.g.* to attend an ATLAS design review that was in fact held virtually, they have been removed. This has only a minimal cost impact in most subsystems.

Tasks that may have been delayed (past or future) for non-COVID-19 reasons such as technical issues are not part of this BCP and may be addressed in future non-COVID BCPs, or may remain as variances.

As noted by NSF, the COVID BCPs have been developed as a means by which to allow the EVM tools to be more effectively used to manage the project, in particular by adjusting past and near-term tasks to more accurately reflect the schedule in light of COVID related delays. This COVID BCP does improve the effectiveness of the EVM tools to manage the project in the following ways:

- The Project Office uses the baseline schedule cost profile at the institutional level to generate the funding allocations to our subawardees. As can be seen in the tables below, the overall effect of this COVID BCP is to move significant funding to later years. Without this adjustment, our funding allocations would be simply incorrect in many cases, and would require developing a new method by which to determine the allocations.
- While the overall project (*i.e.* WBS Level 1) cumulative SPI seems to have been somewhat stable over the past few months, it masks the fact that the SPI at the more detailed levels is not stable in many instances. Removing the COVID impacts on the SPI at all WBS levels allows for a more accurate picture of the technical state of the project at these more detailed WBS levels which may not be apparent in the variance reports at WBS level 3 when COVID impacts are included.
- It reduces the number of variance reports required, making it possible to obtain a quick overview of the technical progress of the project without the need to disentangle the COVID components of the schedule delay.

- The L2 managers use the SPI to monitor the schedule. Again, eliminating the COVID impacts that mask the true technical SPI does make the tools more effective for the management of the project by the L2 managers. Technical schedule issues stand out more clearly without the COVID impacts potentially dominating the variance report.

An analysis of the COVID-19 cost impacts by sub-system before and after this BCP are broken down by cost “type” and are shown in the following table (in \$).

Row Labels	DIRECT	FRINGE	OVERHEAD	ESC	Grand Total
After	39,451,087	3,271,441	4,544,850	4,099,938	51,367,316
6.04.01 FE Electronics	5,035,746	529,656	378,295	308,708	6,252,404
6.04.02 FEB2	6,016,641	590,482	45,964	926,852	7,579,940
6.04.03 BE Electronics	4,864,805	163,120	579,517	478,333	6,085,775
6.05.01 Main Board	2,657,558	3,491	46,342	103,595	2,810,985
6.05.03 ELMB	180,459	19,173	55,400	21,223	276,256
6.05.04 Low Voltage Power Supply	1,297,966	98,589	186,691	131,783	1,715,029
6.06.01 sMDT	3,774,146	496,015	869,528	353,206	5,492,895
6.06.03 TDC	793,747	145,232	170,349	92,530	1,201,858
6.06.04 CSM	2,116,599	102,448	121,449	153,091	2,493,586
6.06.05 LOMDT	3,086,754	361,434	402,664	368,573	4,219,425
6.08.01 LO Calo and FOX-F	239,907	44,275	49,008	49,916	383,105
6.08.02 Hardware Track Trigger Processing	6,673,232	245,619	391,244	631,843	7,941,938
6.08.03 Global Event Processor	2,446,195	404,485	1,176,247	442,565	4,469,491
6.08.04 EF Tracking	267,332	67,422	72,154	37,720	444,628
Before	38,997,027	3,199,421	4,434,227	3,849,255	50,479,930
6.04.01 FE Electronics	4,982,442	520,139	368,212	293,069	6,163,861
6.04.02 FEB2	5,934,191	568,507	45,964	850,659	7,399,322
6.04.03 BE Electronics	4,752,964	155,221	555,666	425,197	5,889,047
6.05.01 Main Board	2,632,235	3,491	46,342	100,248	2,782,316
6.05.03 ELMB	180,459	19,173	55,400	21,223	276,256
6.05.04 Low Voltage Power Supply	1,297,966	98,589	186,691	122,679	1,705,925
6.06.01 sMDT	3,774,146	496,015	869,528	349,121	5,488,811
6.06.03 TDC	793,747	145,232	170,349	86,585	1,195,913
6.06.04 CSM	2,109,866	100,428	119,173	118,379	2,447,845
6.06.05 LOMDT	3,038,295	350,611	393,791	351,543	4,134,239
6.08.01 LO Calo	239,907	44,275	49,008	49,916	383,105
6.08.02 Hardware Track Trigger Processing	6,673,232	245,619	391,244	631,843	7,941,938
6.08.03 Global Event Processor	2,346,018	395,034	1,120,094	415,290	4,276,437
6.08.04 EF Tracking	241,559	57,088	62,766	33,503	394,916
Diff					
6.04.01 FE Electronics	53,304	9,516	10,083	15,639	88,543
6.04.02 FEB2	82,450	21,975	0	76,193	180,618
6.04.03 BE Electronics	111,841	7,900	23,851	53,136	196,728
6.05.01 Main Board	25,323	-	-	3,346	28,669
6.05.03 ELMB	-	-	-	-	-
6.05.04 Low Voltage Power Supply	0	-	(0)	9,104	9,104
6.06.01 sMDT	(0)	(0)	(0)	4,085	4,085
6.06.03 TDC	0	0	(0)	5,945	5,945
6.06.04 CSM	6,733	2,020	2,276	34,712	45,741
6.06.05 LOMDT	48,459	10,823	8,873	17,030	85,186
6.08.01 LO Calo	-	-	-	-	-
6.08.02 Hardware Track Trigger Processing	-	-	-	-	-
6.08.03 Global Event Processor	100,176	9,451	56,153	27,275	193,055
6.08.04 EF Tracking	25,773	10,335	9,388	4,217	49,713
Total	454,060	72,019	110,624	250,683	887,385

For reference, we provide a summary of the “before and after” profile cost changes (in \$) by subsystem below. This table is available in the BCP documentation.

Row Labels	FY20	FY21	FY22	FY23	FY24	FY25	FY26	Grand Total
After	2,165,205	6,509,749	8,983,840	11,335,895	7,466,020	13,383,848	1,522,758	51,367,316
6.04 LAr	583,577	1,813,848	3,017,132	3,532,419	3,198,489	6,384,818	1,387,837	19,918,119
6.05 Tile	292,067	1,177,937	1,369,125	1,488,294	377,080	97,767		4,802,270
6.06 Muon	878,657	2,582,990	2,895,666	4,529,142	1,998,942	522,367		13,407,764
6.08 Trigger	410,904	934,974	1,701,917	1,786,040	1,891,510	6,378,897	134,921	13,239,163
Before	2,166,967	7,541,920	12,143,140	7,422,918	8,089,183	12,702,619	413,183	50,479,930
6.04 LAr	583,577	2,007,321	4,937,101	1,529,474	4,153,882	5,962,614	278,262	19,452,231
6.05 Tile	293,829	1,490,712	1,301,603	1,362,384	293,649	22,319		4,764,497
6.06 Muon	878,657	3,049,303	4,364,951	2,736,222	1,832,216	405,458		13,266,808
6.08 Trigger	410,904	994,585	1,539,484	1,794,837	1,809,436	6,312,228	134,921	12,996,395
Diff								
6.04 LAr	0	(193,473)	(1,919,969)	2,002,945	(955,393)	422,204	1,109,575	465,888
6.05 Tile	(1,762)	(312,775)	67,522	125,910	83,431	75,448	-	37,773
6.06 Muon	(0)	(466,313)	(1,469,285)	1,792,920	166,725	116,909	-	140,956
6.08 Trigger	-	(59,611)	162,433	(8,797)	82,074	66,669	-	242,768
Total	(1,762)	(1,032,172)	(3,159,299)	3,912,977	(623,163)	681,230	1,109,575	887,385

In the following section we describe the COVID-19 changes by subsystem.

WBS 6.4 Liquid Argon Electronics

Overall, the COVID-19 impacts are due to: lab personnel absences due to positive COVID tests or exposures; unavailability of commercial electronics components due to the worldwide ASIC shortage; prolonged delivery times for bare PCB fabrication and also assembly due to increased demand as well as COVID-related staffing issues at vendors, and reduced efficiencies during these periods due to childcare issues, lack of direct collaboration as a result of travel restrictions, etc. Below we provide a description of the COVID-19 impacts at the deliverable level (WBS level 3). Of the \$466k cost increase for LAr, \$145k is due to escalation as a result of the COVID-related delays, which are typically around 9 months. Here is a more detailed breakdown at L3 of the remaining \$321k.

6.4.1 Front-End Electronics (FEE)

LAr ADC Development: Due to delayed radiation tests and lower work efficiencies, the COLUTAv4 ADC ASIC submission was delayed until September 2021, over 9 months behind the original schedule. Packaging of the ASICs once received, as well as fabrication and assembly of the test board, all took longer than usual, due to electronics supply chain issues related to the great increase in global demand. Work absences of lab personnel due to Omicron infections further slowed down the progress. Testing of the COLUTAv4 ADC ASIC finally got underway in February 2022.

The cost increase is due to ~0.5 FTE in additional manpower needed at UT Austin for ADC testing, to account for accumulated COVID inefficiencies.

Optical Link Development: COVID-related inefficiencies, mostly at CERN, delayed submission of the lpGBTv1 ASIC until April 2021, delaying the start of lpGBTv1 testing at CERN by about 5 months. Additional delays were incurred before sample chips could be received at SMU and testing could start there.

The cost increase is due to ~0.4 FTE in additional manpower needed at SMU for optical link testing, to account for accumulated COVID inefficiencies.

6.4.2 Front-End Board (FEB2)

Assembly of additional Slice Testboards was delayed until September 2021 by the lack of the required custom LAUROC preamp/shaper chips from our French colleagues; the chips were not available due to a combination of administrative delays due to previous COVID shutdowns of the French labs involved, plus

packaging vendor delays related to the worldwide ASIC shortage triggered by COVID. After a number of months of investigations that eventually eliminated various other possibilities, it was concluded that the problem with the new Slice Testboards is that the LAUROC ASICs are damaged. Since all the LAUROC chips were individually tested by our French colleagues, the only feasible explanation is that they were damaged during PCB assembly. This problem was discussed with the assembler, who stated that they properly followed all their usual procedures, including backing the chips before assembly, etc. However, unfortunately the evidence shows otherwise. We will likely never know exactly what went wrong in the assembly process. Given that we have years of excellent and trouble-free experience with this assembler on various projects, for both prototyping and larger scale production runs, the fact that something was messed up during the height of COVID is telling. We can only speculate about whether it was due to them having some of their more experienced people missing due to COVID, or bringing in new people either as replacements or to expand their capability to meet the huge increase in demand in recent times due to COVID. An additional indication that they are being impacted by COVID is that a recent job took several weeks longer than usual, which they attributed to capacity issues.

The defective boards are being sent now for rework, by replacing damaged LAUROC chips with the limited spares available. Once repaired, the boards will have to be retested before being sent to international collaborators for the performance of the various lab tests that have been planned.

The cost increase is due to ~1 FTE in additional manpower at Columbia for Slice Testboard testing, to account for accumulated COVID inefficiencies plus the need to repeat some tests after a few boards, that were damaged due to COVID-induced issues at the assembler, are repaired.

6.4.3 Off-detector Electronics (BEE)

Delivery of the Xilinx Zynq FPGAs needed for making prototype SRTM boards and SRTM test boards was delayed by about 9 months and had a cost increase of about 50% due to the global shortage of complex ASICs. The needed Zynq chips were finally received at the end of December 2021, and board assembly is now underway. The PCB assembly is taking a few weeks longer than usual due to COVID-related supply chain issues, namely enormously increased demand for electronics production. In addition, efficiencies were reduced as several personnel had to isolate due to either positive COVID test results or close exposures during the Omicron surge of COVID.

There is a ~\$44k increase in direct M&S costs, due to a ~50% increase in the cost of Zynq FPGA chips resulting from the global ASIC shortage problem. There is an additional cost increase due to a ~0.6 FTE increase in manpower working on hardware at SBU and a ~0.6FTE combined increase in firmware manpower at UAz and NYU, due to accumulated COVID inefficiencies.

WBS 6.5 Tile Calorimeter Electronics

6.5.1 Tile Calorimeter Main Boards

Production of the Tile Calorimeter Main Boards (WBS 6.5.1) has a material cost increase of \$25,480 of which \$25,323 due to the 10% COVID logistics tax imposed by the electronics distributor to cover COVID shipping cost increases, and the rest from escalation of delayed board assembly.

The labor increase of \$2,880 is due to the escalation of delayed tasks due to COVID. The delayed tasks are the production cycles, which are only delayed by 2 months, but that pushes the entire chain across annual escalation dates.

6.5.3 ELMB-Motherboard

There are no COVID-related delays to this deliverable.

6.5.4.1 Tile Calorimeter LVPS Bricks

The increase of \$9k is all from escalation of material cost and labor due to a delay in preproduction.

WBS 6.6 Muon System

The COVID impact in this BCP for the Muon System has led to delays (3-6 months). Due to inefficiencies in work, as well as COVID-related delays impacting our international partners, many tasks have taken longer than expected – therefore some increases in resources have been requested to account for the additional work required.

6.6.1 sMDT

Tasks SMDT630365, SMDT63065T, SMDT630440, SMDT630440T (travel to CERN and testing of chambers at CERN) were removed because the chambers are being stored in a warehouse before being sent to CERN in a larger shipment (half of the chambers) later in the year. The corresponding effort and travel was added to tasks SMDT630580 and SMDT630580T to reflect the additional effort and time to test the chambers at CERN at that time. The cost increase is only due to escalation.

6.6.3 TDC

The overall schedule for the pre-engineering run was delayed due to COVID inefficiencies for our engineer. There was limited access to the lab and other facilities. We also had test results cross-checked by the MPI group and their engineers also suffered from COVID inefficiencies and lab access. We relied on new prototype mezzanine cards from MPI to perform some tests and fixes we proposed, but it took longer to have these cards fabricated and assembled due to COVID-related delays. The cost increase is due entirely to escalation.

6.6.4 CSM

Pre-production, large-scale test stand construction, and integration testing were delayed. All were due to COVID inefficiency in work rate - our engineer working from home with limited accessibility to the lab. She is also working from home with a child who cannot be sent to daycare due to health concerns connected with COVID. The cost increase shown for this deliverable is due to some extra labor required to make up for COVID-related inefficiencies and escalation. The schedule is also shifted because of supply chain issues for some components, which we assume are connected to COVID.

6.6.5 LOMDT

In the past 9 months covered by this COVID BCP, delays of ~1.5 calendar months have continued to accumulate due to: the inefficiency of teleworking with team members spread across a 9-hour time zone; face-to-face workshops that could not take place; people getting sick; and childcare. Some of the work has also been slowed down by board repairs taking much longer than expected due to vendor COVID-induced delays. In addition, the fabrication of the prototype has partially been delayed due to COVID, and we expect an additional ~2 months delay in its production later this year due increased lead time in components delivery, including the FPGAs for which the order was placed in summer 2021. Consequently, the upgrade of the test benches for the prototype have been delayed.

The update to the schedule to account for COVID related delays allows us to disentangle them from actual project delay. The cost impact of the addition of ~1.5 calendar months to the schedule, corresponding to 0.42FTE total, is \$85k where \$17k are from escalation before overhead cost.

WBS 6.8 Trigger

WBS 6.8.1: L0Calo Fiber Optic Plant

There are no COVID-related delays to this deliverable.

WBS 6.8.2: Hardware Track Trigger Processing

There are no COVID-related delays to this deliverable.

WBS 6.8.3: Global Trigger Firmware

The primary driver for changes to this WBS continues to arise from delays in hiring engineering effort due to COVID-related restrictions in hiring at universities. In addition, the availability of existing engineers was reduced due to COVID-driven loss of engineering staff. In particular, Chicago and Oregon suffered from continued hiring challenges and the Pittsburgh group lost an engineer who left the US over COVID concerns. Once personnel were hired, in some cases there have been longer ramp-up times due to COVID-related travel restrictions and the inability to meet in person. In general, discussions of interfaces and specifications have been more drawn out and it has been more difficult to converge due to the lack of in-person meetings.

The currently-delayed tasks in 6.8.3.1, 6.8.3.2, 6.8.3.3, 6.8.3.5, 6.8.3.6, and 6.8.3.7 were extended to accommodate a realistic schedule for their completion. A small amount of additional labor was added to allow these delayed tasks to be closed out. A correction was also introduced in 6.8.3.1 to compensate for an unanticipated side effect of previous COVID BCPs (stretching of task durations without adding sufficient effort); additional effort was added to correct for this. The total added effort in 6.8.3.1 was \$119,411.

The total change in cost due to additional labor and delayed task escalation was \$193,055. Factorizing the impacts due to COVID allows us to distinguish between COVID and non-COVID impacts on the project, and thus we can better track and manage the non-COVID effects on these Global Trigger Firmware algorithm deliverables.

WBS 6.8.4: Event Filter Tracking

A correction was introduced to compensate for an unanticipated side effect of previous COVID BCPs impacting 6.8.2 (stretching of task durations without adding sufficient effort). Additional effort in the amount of \$49,713 was added to 6.8.4.1 to correct for this.