Report of the II ATLAS Phase-II Upgrade Project Review (P2UG)

ATLAS-P2UG Meeting, 4-7 May 2020

In-Depth Review: ITk-Strips, LAr, and Muon projects
Regular Review: TDAQ, ITk-Pixels, ITk-Common and Tile projects

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Process

After the P2UG review in Nov. 2019, the P2UG met again with the Upgrade Coordinator (UC) and the deputy Technical Coordinator on Feb. 11th for the intermediate status update video meeting. Besides examining the general progress and the milestone completion report, the P2UG was informed about the progress made in addressing the recommendations issued during the Nov. '19 review (GE-1 through GE-5, TD-1, TD-2). The P2UG found that significant progress had been made in all directions and, after having received further explanations from ATLAS in written form, submitted a note summarising the conclusions to the LHCC chair.

Due to the exceptional measures taken worldwide to combat the COVID-19 epidemic, the P2UG review in May was then organised in collaboration with the ATLAS UC as a set of video-conference meetings held from the 4th to 7th of May'20, but limited to the afternoons (CERN time) to facilitate the participation from colleagues in both US and in Europe.
As usual, ATLAS made available in advance a milestones snapshot (taken on April 1st), the summary report of the last internal reviews and the recently updated Risk Register files. The P2UG, after examining the documentation, sent to ATLAS a list of requests for clarifications to be provided during the review.
The first day of the review was taken by the plenary session, with the general presentations by the UC and by all the projects, while the second day was dedicated to the ITk-Strips, the LAr and the Muon drill-down parallel sessions. On Wed. the 6th, the P2UG met with ATLAS management and, after receiving feedback in written form on several questions, convened in an executive session for the rest of the day. The preliminary feedback from the review was presented to ATLAS in the closeout session on May 7th.

Despite the inconveniences of meetings carried out with most participants participating from their homes, the review run pretty smoothly.
The very effective cooperation of the ATLAS UC and P2 upgrade project teams in providing the material and the presentations in advance, as well as in responding with quick and thorough feedback to our requests was essential to the review process. The P2UG congratulates all the speakers for the quality of their presentations and the UC and the project leaders for the organization of the material presented in the drill-down sessions that made it possible for the committee to capture, in a few hours, a very comprehensive and clear picture of the status of the various activities.

General observations, comments and recommendations

It emerged quite clearly from the review that the COVID-19 pandemic had already made considerable impact on the schedule of all projects and the milestones achieved. The P2UG commends the project teams for their efforts in coping with the difficult and unique situations they have been facing in the last few months: even some ASIC

developments and lab activities were able to proceed at home despite the closure of laboratory facilities everywhere.

The schedules for reopening universities and laboratories were not at all clear at the time of the review, so it was not possible to make a realistic overall evaluation of the impact of the epidemic on the schedule of the projects. ATLAS had assumed a nominal 3 months delay on activities when no better estimate was available. We aim at being able to make a solid assessment of the P2 project schedules in the November review, once a stable mode of operations of research institutions and industrial partners has been re-established.
Particularly concerning are the delays caused by the unavailability of the irradiation and test facilities in a time when crucial ASICS developments are being carried out and are requiring important validations before proceeding to production.

Schedule assessment

As announced in the February intermediate meeting, ATLAS performed a general schedule assessment with the help of external consultants that led to the definition of a work program aimed at:

- developing and providing a consistent scheduling standard across the projects and
- delivering a fully functional integrated ATLAS Phase-II schedule.

Such a program was carried out for all the projects to be reviewed in detail in May (ITk-Strips, LAr, Muon) with the expectation of completing the structural changes for all the other projects by mid-May. A structure for high level milestones including dates for installation and commissioning, as well as for external and for project-to-project interface milestones, has also been setup. ATLAS should therefore soon have the possibility of properly evaluating the critical paths and consistently assessing across projects the schedule contingencies.

We congratulate ATLAS for having addressed with determination the schedule shortcomings and inconsistencies raised during the Nov. 19 review and further highlighted by the analysis carried out in cooperation with the external consultants. In particular, we are looking forward to seeing the outcome of the ITk-Pixels current schedule revision work and we encourage again the project to explore all possibilities to mitigate the delays, in particular through a possible optimisation of the ITk-Pixels production phase.

The P2UG also welcomed the recent efforts to strengthen the ATLAS internal review organisation and to more precisely define the outcome and the follow-up of the reviews. We hope that this will help to complete efficiently the rather dense program of reviews scheduled to take place in the coming months.

Schedule status

Despite the efforts to mitigate the impact of accumulated delays and the incorporation in some projects of the additional contingency granted by the new LS3 shutdown dates, the overall ATLAS P2 upgrade schedule looks more problematic than ever. Most concerning is the realisation that the re-baselined schedule of the ITk-Strips, taking into account COVID-19, is now showing approx. 4 months of float for the detector and a negative float for the services. No float exists anymore between the ITk-Pixels completion date presented in Nov. 19 and the moment when the detector is needed for integration in the updated LS3 planning.
We also learned, during the review, that the ITk-Pixels Services PDR follow- up work will require a further period of several months to be completed and it is coupled to the decisions on the implementation of the Regional Readout and L0/L1 options currently under evaluation.

While we were glad to see that the working groups, that should provide the rationale for such decisions, have started their activities, we are concerned about the time it may take for them to converge - we have noted that the first step of this critical process (RR recommendations) has been delayed by two months with respect to the planning presented at the P2UG intermediate meeting, in February. We strongly support the ATLAS commitment to arrive at a first decision in June, hence enabling the ITk-Pixels project to overcome the current design uncertainties. The P2UG is available to have a special P2UG Vidyo meeting in late June or early July for an update on the process.

ASICs developments

The exploitation of the CERN CHIPS initiative by ATLAS P2 projects seems to be gaining some real possibility of materialising and we strongly support the effort, as well as the attempts to address the risk of manpower erosion in RD53. The success of these ASIC developments is key to the timely completion of the projects.

Recommendations

GE-1) We would suggest that ATLAS make as soon as possible a survey of the future availability of the various laboratory facilities and keep it up to date, while organising some possible mitigation actions.
GE-2) In the coming months, once the impact of the COVID-19 epidemic can be quantified, all projects should consider re-baselining their schedule so that by the November review a consistent picture of where the projects stand may be evaluated.
GE-3) The consolidation of the schedule and the inter-linking of ITk subproject schedules is of high importance for the overall project. For the November P2UG review, an updated project schedule with verified interlinking across the sub-projects and solid and reliable critical path indicators is expected.

Milestones

The status of milestones completion, updated on Apr. 1st, and the progress in the last reporting period (Jan. 1st - Mar. 31th 2020) are summarized in the following table:

Project	*All*					*Expected to be completed in the reporting period (Jan.1st- Mar. 31th)*		
	Tracked by P2UG	*Completed*	*Completed over Tracked*	*Delayed*	*Average delay (months)*	*Tracked by P2UG*	*Completed*	*Completed over Tracked*
TDAQ	165	4	2.4%	9	7.9	8	0	0.0%
ITk-Strips	212	19	9.0%	185	4.7	13	5	38.5%
ITk-Pixels	340	8	2.4%	322	4.9	17	1	5.9%
ITk-Common/DB	70	11	15.7%	24	5.7	9	0	0.0%
LAr	87	13	14.9%	42	3.6	5	1	20.0%
Tile	112	26	23.2%	11	4.0	11	4	36.4%
Muon	142	24	16.9%	105	6.8	15	3	20.0%
TOTAL	1128	105	9.3%	698	5.1	78	14	17.9%

The table shows the impact of the COVID-19 pandemic with a large part of the milestones due in the reporting period now postponed.

Projects in-depth review

ITk-Strips

The ITK-Strips team presented a comprehensive review of their activities since the previous P2UG review in May 2019, showing steady progress in most areas, while also some risks and areas of challenges realised. The team also presented a new schedule, having undergone baseline changes and statusing, developed in consultation with the ATLAS PMO and Manta Ray Consulting. Our findings, comments and recommendations are itemized below.

Observations

- The ITK-Strips has seen significant advancement in most of the project areas since the last in-depth review in May 2019. There has been 1 PRR and 9 FDRs (some conditionally passed or passed with recommendations).
- The project is entering the pre-production phase. Procurement activities are advancing, including sensors and ASICS - nearly 50% of the pre-production sensors are delivered.
- Some risks have been realised: SEE is seen in all three FE ASICS. After significant design modifications and endorsed by ASIC FDR part II, the ABCstar has been submitted with delivery expected in late May. The AMACstar and HCCstar chips are still in design for mitigation of the SEE issues, with the ASIC FDR part III planned in June. The submission of HCCstar is expected in mid-summer at the earliest.
- Tests of fully loaded electrical Long Staves have revealed a significant temperature-dependent increase in the noise level. This remains an open issue, although progress has been made in identifying the source of the effect. The investigations continue but are delayed by the current pandemic. Tests of Short Staves are on-going and similar effects are expected in electrical petals yet to be tested.
- ITK-Strips schedule has had a baseline change, addressing the delays in the FE ASICs delivery and the CERN ESE chips, along with a mitigation plan to gain back some of the lost time in the production process. After schedule statusing, assuming a maximum of 3 months delay due to COVID-19, the system float is now reduced to 111 days.

Comments

- The progress on nearly all fronts of the ITK-Strips project is very impressive and the team should be congratulated. The team is now focused on managing the pre-production process, with a carefully drawn plan to reduce the impact of the various foreseen delays in the schedule.
- The current plans for pre-production activities, including procurements, do not yet address the potential long-term effect of the shutdowns due to COVID-19. The schedule includes only the nominal 3-month delay, awaiting better understanding of how the situation will evolve at CERN and in the collaborating countries.
- The delivery of the CERN ESE chips and the SEE issues in the FE ASICS remain very concerning. The outcome and the timing of the tests of the ABCstar from the latest submission as well as the conclusion of the SEE mitigation in the AMACstar and HCCstar chips- and subsequent tests after submissions, are among the most important drivers of the schedule. Any further need for chips submissions would likely remove the remaining float in the schedule.

Recommendations

ST-2) Given the possibility of a prolonged period of restrictive activities due to COVID-19 in most participating countries in the coming months, the committee supports the ATLAS intention to re-evaluate the impact on the schedule in the late summer and to rebaseline the project. Delays significantly longer than the 3-month introduced provisionally, may eventually suggest a different optimum for deployment of resources that would require a careful evaluation.

LAr

General Observations/Comments:

Ignoring the effects of COVID-19, all work packages are ~ 3-4 months behind the schedule but the float is still large.

All elements (PA/SA, ADC, …) of front-end electronics have progressed well even if all the measures of performance have so far been achieved in "ideal" laboratory conditions.

The R&D schedule, especially for what concerns some radiation tests, is being impacted by the COVID-19 crisis and is linked to the restart of accelerator facilities, not only at CERN.

The new LVPS architecture is an important improvement, but the priority now is to test the performance of the integrated system which is planned as the FEB2 'slice test'. The LVPS is built with long cables and POL which may induce noise in the PA/SA and in the ADC. The validity of the new architecture of LVPS must now be proven with the slice test (e.g. induced noise, EMI, adequate LV stability, cross talk etc). These studies should also have an impact on the decision that needs to be made between the powering options (24 V/48 V).

General Recommendations:

LA-1) The successful execution of the slice test should be a precondition to pass the component PDRs. This is especially important for the new architecture of the FEC LVPS for which a system test is mandatory.

Sub-project specific Observations/Comments:

Front-End electronics

Since the HEC version of the PA-Shaper is now based on the LAUROC, it was reassuring to know that eventually the development is agnostic to the choice between LAUROC and ALFE.

For the ADC, there will be a schedule delay in the event of the `IP block' option being chosen (based on existing CMS chips), but the global impact should be contained in less than 6 months and with no CORE cost impact.

We consider the Slice Test to be a major step for the FEB project, as it will require the inter-connection of the subsystems and allow the consequences on the system

performance to be studied. We were not clear whether a corresponding Slice Test for the HEC setup is foreseen but this would clearly be a good idea and should also be considered.

Calibration system

As the chosen technology has a long turn-around time, but has already been demonstrated to be radiation hard, we feel that it might be reasonable to go ahead with the submission of the CLAROC v3, even if the TID tests have not been carried out.

LV Power Supplies

Even though sufficient numbers of LTM4169 devices have been purchased to complete the project, with contingency, we understand that these components are no longer produced. It would be prudent therefore to invest some time now to, at least, identify a suitable replacement that could be used if needed.

The ELMB2 choice is now supported by CERN and this has solved one of the main issues. Implementation is now more a matter of "negotiations" with the technical coordination.

Recommendations:

LA-2) Define for both for LAUROC Vx and for ALFEx the requirements on LV performance and the process dispersion. A sufficient number of LAUROC2 and ALFE2 ASICS should be tested to verify that the running input voltage needs for the PA/SA chips are uniform across the production process and to confirm that the performance dispersions are acceptable, before and after irradiation.

LA-3) Explore the possibilities to plan irradiation tests of the complete FEB2 setup, even if all of the parts (subsystems) are qualified radiation hard. We understood that this is going to be rather difficult, but it should be considered.

LA-4) FPGA resources in the LASP are already close to fully-loaded and this can become an issue. Specifications/Interfaces with other systems as the global trigger, DCS, etc. represent a critical aspect of the design and we advise tight management to keep the project on track.

LA-5) We would like to see a demonstration that the LATS requirements on clock and jitter are reached with the existing design.

Muon

Observations and Comments:

In the Muon system, 15 milestones were expected to be completed in the period, and 3 were completed. Of the uncompleted milestones, most were internal reviews that were delayed, due to the fact that they were all grouped together. We therefore support the plan to split the RPC PDR into three separate PDRs to allow individual reviews to proceed sooner.

The preparation for sMDT chambers production has made good progress and production is ready to begin. The MTD electronics are on schedule, aside from COVID-19 related delays. The delay of the Phase 1 NSW, however, has created a space conflict since the NSW chambers will occupy the space foreseen for storing and testing the new sMDTs.

As recommended at the P2UG review in November 2019, the LV powering scheme was reviewed and LDO regulators were selected over DC-DC converters. The study included a review of the thermal load of the different options, and the heating from the LDOs was considered manageable.

The RPC production schema foreseen is rather complicated and based on activities carried out in many countries and a complex shipment pattern. Therefore the plan appears vulnerable to restrictions in the international movement of goods and people.

In the design of the RPC FE ASIC, a delay of several months accumulated before the COVID-19 outbreak due to the CADENCE license problem in the Italian Institutes and the design work has been further interrupted by the travel restrictions due to the pandemic.

In the TGC electronics design, the name of the board originally intended to replace the SPP was changed to JATHub (JTAG Assistance Hub). This name change reflects a decision to locate the JATHub boards in the HSC VME crates, and opens the possibility of leaving the legacy SPP boards in place as a backup solution for TTC distribution.

To adapt to procurement and bidding requirements, a change was made to the power supply procurement plan whereby the prototype phase is eliminated. In order to maintain the schedule constraints, the production tenders of the power system will move to 2022, to reserve more time for the pre-series qualification.

Recommendations

MU-1) Find additional space for sMDT test and commissioning to avoid interference with the NSW.

MU-2) Explore different solutions to speed up to RPC Front-end ASIC design.

MU-3) Power system: try to minimize the risks that the procurement procedure may result in having to run the muon system with a mixture of different types of power systems at same time. Ensure ample engineering engagement in the specification working group.

Other Projects

TDAQ

General Observations and Comments

The TDAQ project has made significant progress in all areas since the Nov 2019 P2UG meeting. The team should be congratulated on their impressive achievements and on successfully handling the challenges of evolving requirements and boundary conditions in this huge and complex project.

The AM08 chip design is evolving through a series of preparatory reviews, after it had become clear that the original PDR date in December 2019 could not be met. The PDR process is expected to be completed in July. In general ASIC development has slowed down, partially because the software cannot be used in telework, as necessitated by COVID-19 measures, due to licensing issues.

Various milestones are self-delayed by now. In some cases this is due to COVID-19 related issues, others are pending a final decision on the ITk-Pixels readout and services. A detailed decision path on the final track trigger strategy is in place. The whole schedule needs to be re-baselined after all the effects of the LHC schedule and COVID-19 can be taken into account. It is currently expected that there will be a minimum float of about 15 months after the re-baselining.

Sub-project specific Observations and Comments:

The decision path on the track trigger foresees a combination of various digital decisions, like Regional Readout versus standard readout, commodity versus custom hardware, or AM chips versus FPGA-based solutions for track pattern recognition. Not all combinations seem to be equally promising; for example in case of no Regional Readout, a downscoped L1 seems to have little benefit for physics performance. The resource requirements have only been partially explored but are an important consideration for decisions.

In case the decision is in favor of a split hardware level trigger, L1Track commissioning is now foreseen for the beginning of Run 4, which seems very challenging.

The number of milestone self-delays raises the question whether the schedules are realistic. It is not possible to track the project productively without some attention to the reporting metrics.

Recommendations:

TD-1) Although the process is quite advanced, we would recommend ATLAS to consider reducing the track trigger decision path combinatorics to a small number of realistic scenarios. With a full evaluation of both technical and resource needs (human and financial) this could help to arrive at a fully informed decision. This may require a 'global' discussion by a suitably staffed panel, making a final decision, although P2UG is aware that the Regional Readout decision may have to be factorised to proceed at an earlier point for practical reasons. It is understood that this decision process is demanding for

the collaboration, but it is very important that it is carried through now without significant delay, such that the matter can be put to rest afterwards.

TD-2) Resolve the ASIC development by telework situation. It is hard to predict how the COVID-19 situation will evolve long-term, and this ability may not have been needed for the last time.

TD-3) After the June re-baselining, critically examine the schedule, and ensure that rational DCPs are in place everywhere.

An intermediate report in June/July, in particular concerning the Regional Readout decision and the track trigger decision path is considered very useful.

ITk-Pixels

The ITk-Pixels subproject presented an overview of the current status showing substantial technical progress since the last review, for which they should be commended.

Observations:

- The schedule of the subproject is currently being reworked to make it more robust and predictive, particularly for the critical path analysis.
- The subproject is moving to the final design review phase, with 8 FDRs planned (modulo COVID-19) for the September-October time frame.
- In response to previous recommendations, the subproject has strengthened the team and tools to coordinate production flow between the multiple sites involved, as well as rationalised the site grouping based on regions and scope.

Comments:

- It is very good news to see that the ITkPixV1 chip is submitted, that the radius reduction mitigated the services envelope violation at PP1 and that the data transmission scheme has evolved from a design on paper to prototype testing with promising results.
- In general, given the current pandemic, the subproject is doing a good job of making progress wherever possible, although the lack of facilities to validate final design prototypes is concerning (and shared across the HL LHC).
- Given the delays seen already in ASICs and in general the long duration of iteration/resubmission cycles, it is imperative that ATLAS remain on the schedule presented for the HTT decision and potential implications of the Regional Readout as modifications to the pixel chip design are a serious threat to maintaining the overall ATLAS upgrade schedule.

Recommendations:

PI-1) Continue to work with the Upgrade Project Management Office to have a fully reworked and predictive schedule and critical path analysis by the next P2UG review. With a preview in a video meeting preceding the review.

ITk-Common/DB

The ITk-Common subproject presented an overview of the current status showing substantial progress since the last review, for which they should be congratulated. The project achieved 11 out of the 24 milestones in the baseline schedule until Q1 2020 but none in the last reporting period. The delayed milestones are generally far away from the critical path and do not constitute a concern.

ITk-Common Electronics

- The Environmental Monitoring passed SPR follow-up and is preparing a temperature sensor PDR in June, aiming at the delivery of production sensors for strips system tests in December.
- The Interlock FDR and Felix I delivery are slightly delayed, but not critical.
- The Beam Condition Monitor (BCM) project made very good progress after the activity in the project was on hold for one year due to missing resources. The sensor SPR, the sensor PDR and the ASIC SPR were passed in Q1/2020. The project is actively monitoring the constraints arising from the limited space for the pixel services and its impact on the BCM project.

ITk-Common Mechanics

- The subproject is well on-track. A baseline change proposal (BCP) is being prepared to update the schedule to production.
- PRR for Outer Cylinder and Structural Bulkhead were passed in December
- Surface integration: The SR1 layout was fixed in a document that was approved at the end of April. A change in the use of cooling plans was announced: due to a shift in schedule the intermediate use of an Lucasz cooling system is no longer needed rendering some milestones obsolete. The DEMO plant will entirely cover the needs for ITk-Pixels and ITk-Strips. A previously mentioned concern on the limited capacity and/or flexibility to serve both sub-projects does no longer exist.

ITk-Common Production Database

- The database project is entering an important phase with the ITk project entering into pre-production with an extensive use of the database.
- The SPR was passed in September 2019 and it was decided to split the FDR into two parts (front-end with users & back-end with developers). The FDRs are expected after the COVID-19 shutdown with a baseline date in February 2020

Tile

General Observations:

The Tile group continue to make good progress. It was good to see that, since the last review, many of the long-standing technical issues have found solutions. Ignoring the expected delays from COVID-19, all work packages are roughly on schedule and rather far from the critical path.

Specific sub-project Observations/Comments

Mechanics and Tools

All 5 workpackages have now passed the FDR stage. Two PRR's have been passed with two more expected to follow by the end of the quarter. The Mini Drawer Mechanics PRR was passed in Feb. 2020 but opened the question of radioprotection safeguards in place to handle the recycling of the legacy PMT's at the start of LS3. This needs to be followed up with TC in order to ensure there is sufficient slack in the schedule in the event that PMT activation exceeds CERN safety limits.

On-Detector Electronics

PDR's have been completed for all four work packages. In addition, two FDR's are complete with one more expected by the summer this year. The FDR for the PMT HV dividers was passed but lifetime testing of the boards has been requested to be built into the QC before PRR approval can be given. The FDR for the front-end `FENICS' board has been held up by around 9 months (to June'20) in order to study how best to extend the dynamic range for coupling to the new PMT's. A solution giving a 20% increase has now been demonstrated, with minimal changes to the system. Another issue with negative pedestals looks to be solved but a demonstration on a larger sample of boards is needed before going ahead with the FDR – this requires renewed access to labs. Issues with single event latch-ups seen with v5 of the Daughterboard (which transmits digital data to the off-detector electronics), has been solved by moving to a different FPGA and providing overcurrent protection. The FDR is now scheduled for 2021.

Off-Detector Electronics

All three workpackages have completed a PDR but there is an important follow-up needed to demonstrate that the fast link (10 Gb/s) works between the processing modules (CPM) and the interface with the trigger and FELIX (TDAQi). There is a reasonable chance that a material change to the Carrier Board will fix the issue or else other solutions involving design changes will need to be explored. The TDAQi also needs to look again at the choice of FPGA with a view to reducing the power and resource budget.

Low Voltage System

One PDR still to complete for the LVPS Services has been held up by delays in finalising the LV system architecture – now expected in June '20. The LV bricks had two components fail the NIEL tests at high safety factor. Previous tests suggest these components can comfortably survive the HL-LHC fluence at the required (lower) safety

factor and so a single-batch purchase is being set up. The motherboard that houses the ELMB2 needs to complete the PID test and is waiting for the restart of the CERN CC60 facility.

High Voltage System

Of the four work packages, the PDR for the HV supply board is still missing but a full size prototype is expected in June. A vertical slice test of the full HV chain will feed into the FDR's and could still happen this summer if access to the lab is restored.

Calibration

The Cs calibration control electronics will now be based on the ELMB++ replacement (EMCI) and work is on-going to interface with EMCI and demonstrate radiation hardness. Further progress is currently being held-up by COVID-19.

Recommendations:

TI-1) We urge the Tile Group to push wherever it is possible during the COVID-19 closures, to answer whether a new board material can fix the current issues seen with the high speed link to the TDAQi. Although there is a comfortable float, design changes can be lengthy and progress is not easy in the current climate.

TI-2) We encourage and support linking the HV FDR's to the outcome of an integrated Vertical Slice test of the full HV chain.

TI-3) A Baseline Change Proposal and associated milestone(s), is now needed to track the development of the Cs calibration electronics based on the new EMCI.

TI-4) Simulation studies should be made (if they don't already exist) to estimate the expected activation of the PMTs to be recycled. This can in turn inform evaluating the effect of radio-protection processes on the LS3 schedule.

Follow-up

We would appreciate if ATLAS could give us an update by middle July on the progress in coming to a decision on the RR and the L0/L1 implementation strategy (r. TD-1). At the September intermediate meeting, we expect to be informed about the status of the schedule re-assessing and re-baselining activities of all projects (r. GE-2, ST-1, PI-1, TD-3).