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Report of the ATLAS Phase-II Upgrade Project Review (P2UG)

Fifth ATLAS-P2UG Meeting, 3-6 May 2021

In-Depth Review: ITk-Strips, LAr, Muon, HGTD projects

Regular Review: TDAQ, ITk-Pixel, Tile projects

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The agenda and presentations can be found here:
https://indico.cern.ch/event/1008943/

Introduction

Since the last in-depth review in November 2020, the P2UG has met twice with the ATLAS management. An intermediate update meeting was held on 16th February, addressing the recommendations of the last in-depth review. An extended introductory presentation on the HGTD was also given, since the current meeting was the first P2UG review of this project. The full in-depth review of the ITk-Strips, LAr, Muon, and HGTD projects was then held from 3rd – 6th May.

This review followed the established format of material posted in advance, and then a first day of summary talks from the upgrade coordinator, and from all projects. The following two days were then focussed on the in-depth topics, with further meetings and close-out sessions on the fourth day. However, it is becoming clear that the pace of development on each project is such that a one-year gap between in-depth reviews may not be adequate to follow events and advise the collaboration properly. A current example for ATLAS is the evolution of the TDAQ project, where critical decisions have already been made, and further such decisions are in progress, in the intervening period between reviews. This was addressed by the additional of a supplementary Q&A session with the non-in-depth projects. LHCC may wish to consider whether the format and frequency of P2UG meetings should be reconsidered. It is likely that an additional ATLAS P2UG meeting in July will be needed to receive specific information on the progress in pixels and TDAQ planning.

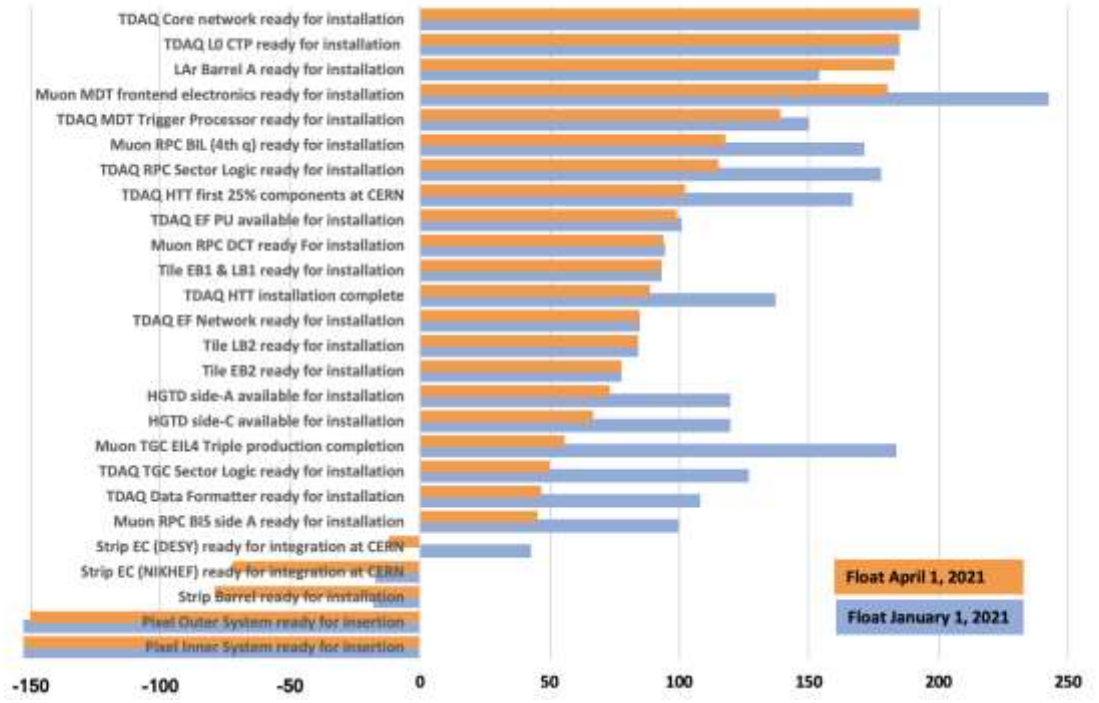
As P2UG has come to expect, the materials presented by ATLAS were comprehensive, transparent, and overall well-suited to the task of judging progress and upcoming challenges. In particular, we thank the upgrade coordinator, resource coordinator and their teams for the ongoing improvements in the formal project tracking tools, and the methods of presenting necessarily complex information.

Progress against schedule

Two key sets of progress metrics are shown in figures below:

- The completion to date of P2UG reporting milestones up until 2021-03-31 (these are an indicative subset of the full ATLAS project milestones), along with progress in the last quarter (2020 Q1) on both expected and previously delayed milestones.
- The current distance-to-critical-path of the tightest milestones, where zero DCP represents delivery exactly on the date required by the LS3 installation schedule.

Project	Baseline Overall (until 2021-03-31)				Baseline Reporting Quarter (Jan-Mar 2021)			Expected milestones from previous report		
	No. P2UG Milestones	No. Expected	Completed	Completed (%)	No. Expected	Completed	Completed (%)	No. Expected	Completed	Completed (%)
1. TDAQ	163	16	12	75%	1	0	0%	3	1	33.3%
2.1 ITk-Pixel(*)	340	32	20	62.5%	12	0	0%	10	4	40%
2.2 ITk-Strips(*)	218	67	32	47.8%	5	0	0%	14	3	21.4%
2.3 ITk-CM(*)	30	7	7	100%	0	0		0	0	-
2.4 ITk-CE	32	18	13	72.2%	4	2	50%	6	3	50%
2.5.1 ITk-PDB	4	2	2	100%	0	0		0	0	-
3. LAr	86	28	21	75%	2	0	0%	3	1	33.3%
4. Tile	114	57	34	59.6%	8	0	0%	5	2	40%
5. Muons (**)	160	73	37	50.7%	9	0	0%	0	0	-
8. HGTD	152	4	3	75%	2	1	50%	N/A	N/A	N/A



It is clear that the direct effects of COVID on the projects have been severe, with few milestones achieved in the last quarter, a worsening situation even from the previous quarter. In the most prominent case (ITK-Strips) around nine months of schedule float have been lost in the last year. On top of this, there are indirect effects of COVID – such as the difficulties in supply chains for ASICs and electronics components – that will continue to affect the project for months or years to come. P2UG is convinced that ATLAS understands where it is at the current moment in terms of project planning. However, it is not clear that they (or any other large-scale construction project) can make an accurate prediction of where they will be in one year's time. It is very likely that the

schedule situation will worsen significantly as the full economic effects of COVID play out worldwide.

In light of the previous view from LHCC that a clear year of schedule float would be appropriate for projects at the current state of development, and observing that more than one project now has a negative float of a few months, it is now clear that the ATLAS schedule is not compatible with the current HL-LHC schedule, nor can it be brought into conformance without significant changes of scope or resources. As reported below, ATLAS is taking positive and proactive steps to address this, in parallel with continuing to try to keep the schedule wherever possible – but projects cannot proceed much longer without overarching schedule decisions being taken.

ATLAS made a clear statement at the in-depth review that they would consider the minimum adjustment to the LHC schedule to allow completion of the project at full scope and with acceptable risk, as a twelve-month extension of Run 3, followed by a six-month extension of LS3. P2UG agreed that this seems feasible in terms of restoring sufficient float in the schedule, but also pointed out that any such decision will necessarily have the effect of transferring cost and risk elsewhere, and could only be made in light of a full appraisal of alternative options. It must be emphasised that a complete replanning of the project schedules would be premature at the current time, since the full medium-term effects of COVID are not yet understood.

General comments

Notwithstanding the schedule challenges, it is very clear that all projects are being pursued with vigour, that progress is being made in every area, that tactical adaptations are being made to project to deal with the immediate COVID situation, and that the project remains under highly effective leadership. The collaboration is not afraid to change its plans or make hard and radical decisions where needed, as evidenced by ongoing fundamental discussions on the scope of pixels and TDAQ.

As the situation evolves over the coming year, it is clear that the importance of, and load on, the upgrade project office will become substantial. It is vital that ATLAS works to optimise the schedule globally, and the metrics above indicate that the situation across projects varies substantially. It is also important that lessons learned and successes achieved in one area are communicated to others.

General recommendations

To ATLAS:

GE-1: ATLAS should continue to investigate ‘adiabatic’ ways of optimizing and accelerating schedules whilst preserving current scope, and without diminishing quality controls or substantially increasing risks.

GE-2: ATLAS should continue its exploration of staging, phasing and – in the worst case – descoping scenarios to bring the schedule closer to target. These explorations should at all points maintain a full, and preferably quantitative, awareness of the impacts on the long-term physics programme of the experiment, as well as on cost and risks. Such exercises should aim to come to initial conclusions and proposals in late 2021.

GE-3: Schedule planning, including the LS3 installation schedule, should be approached as a global optimization. Although it is premature to begin a wholesale replanning of all projects (since the effects of COVID are not yet known), eventual changes of planning in non-critical-path projects in order to accelerate the schedule as a whole should not be ruled out.

GE-4: ATLAS should ensure that the necessary resources and expertise are available to the project office to carry out the recommendations above.

To LHCC:

LH-1: LHCC should define clearly when further concrete information and planning on stage / phasing / descope is needed from ATLAS in order to inform decision-making on the HL-LHC and experiment schedules.

LH-2: LHCC should consider whether project metrics from ATLAS and CMS are sufficient similar in nature to allow direct comparison of the schedules of the experiments, and make recommendations on any further project status information it wishes to receive.

ITK-Strips (in-depth review)

ITK strip project presented in ten hours of presentations and discussions the full scope of its project, the schedule status and delays, technical challenges and risks, the focus in the coming year, and technical progress. The project is commended for accomplishing several major milestones and achievements since the last in-depth review in May 2020 despite COVID. Highlights among those are:

- The sensor PRR was passed in February 2021 and the sensor production order was started.
- The pre-production ABCStar chips were received in May 2020 and SEE tested with promising preliminary results that are however still awaiting full analyses.
- The AMACStar chip FDR was passed in July 2020 and the stave cold noise problem was understood and is no longer a critical issue.
- First End-Cap electrical modules of all types were produced.
- The petal local support core FDR follow-up was passed in December 2020 and the petal assembly contract placed, a first electrical petal was assembled and tested, a first End-Cap wheel was assembled, the Barrel LS and SS bus tape FDR follow-ups were passed in late 2020 and the barrel bus cable pre-production started.

Unfortunately, and mainly due to COVID, significant delays were accumulated and some technical problems arose that are detailed below.

Schedule

The current (Q1/2021) negative float in the ITK strip schedule is -79 working days (3.5 months) against the required delivery date. In April 2020 the float was still positive, at +111 days. This dramatic schedule slip of nine months in one year is mostly (approximately 70%) related to COVID, caused by lock down, reduced efficiency periods in laboratories, and delayed external deliveries. The project leadership estimates that a further three months of schedule slip will be accumulated due to COVID before the November P2UG meeting, which will bring the ITK schedule to an overall six-month overrun by end of 2021.

All subsystems reported COVID-related inefficiencies in order of 30-50%. Out of the 40 milestones scheduled for 2020, 22 have not yet been achieved. The pre-production start date of all components shifted between about 100 and 200 working days. Likewise the anticipated production start dates have moved by 100 to 250 working days. Meanwhile, several items are on the critical path or closed to it, in particular the sensor production, the HCCStar chip design completion and submission, the endcap hybrid and power board tendering, the endcap module tooling and the petal cold tests.

It was found that ITK strip was (and remains) particularly vulnerable to COVID effects due to the highly distributed production model based on several production sites in different countries. COVID hit the project also in the FDR/PRR phase, which needs in particular hands-on activity and

in-person interaction for problem solving and production preparations. This turned out to be very difficult under the current work restrictions, introducing delays in several project areas.

ITK has initiated three major mitigation actions to recover schedule float:

- **Pre-production A/B**: Preproduction has been split into two parts, A and B, with A being 20% of the pre-production using prototype chips (HCCStar/AMACStar). This allows for an earlier start (gaining two months) of site qualification and experience build-up before the remaining 80% of pre-production are launched with pre-production chips.
- **Priming production**: Prior to passing the relevant PRRs, a purchase of 5% of the production HCCStar and AMACStar chips, and hybrid and power board substrates, will be made. This allows production to start immediately after the successful PRR without purchasing delays, and can gain up to six months, but introduced some financial risk. It also requires SEE tests of pre-production ASICS to be completed and modules to show all production specs well ahead of the PRRs.
- **Accelerated production**: Accelerated module production with additional staff and equipment is under investigation. However, sensor production has currently -42 days float and can only be recovered if the sensor supplier can deliver faster than contracted.

The ITK strip project is commended for developing the three proposed mitigation actions. It is understood that possible means to accelerated production have been intensively studied, while it seems too early to initiate an in-depth production schedule review. Such measures should be intensively prepared but will become more effective after site qualifications and first pre-production experiences have been gained.

Comments on subsystems

ASICs

Pre-production ABCStar chips have been available since May 2020 and are showing a high yield (>90%). SEE tests have been performed, but analyses are pending and are expected for the PRR in October 2021. The HCCStar (GF 130 nm process) was re-designed for SEE mitigation, which introduced significant delays has and pushed the chip design and its production onto the critical path. The FDR took place in April 2021 and is has been conditionally passed, allowing a submission in early summer. An alternative chip development, called HCC65 (TSMC 65 nm process), designed as drop-in replacement solution, is ongoing and is planned to be brought up to MPW submission stage in order to mitigate the remaining smaller risk of HCCStar SEE failures. The AMACStar chip passed the FDR in July 2020 and is ready for a common submission with HCCStar. In view of the global 'chip production crisis' a production priming is being anticipated by the project. An agreement is in place with the foundry producing HCCStar/AMACStar covering several productions and negotiations are ongoing to lower the risk of fabrication delays induced by the 'chip crisis', which nevertheless remains a schedule threat.

The very limited number of lpGBT-V0 chips, and the non-availability of lpGBT-V1, is worrisome, blocking the industrialization process of end-of-stave (EoS) card population. This will soon impact on pre-production B if not solved. The support of CERN ESE and the CERN CHIPS initiative turned out to be essential in pushing the recent ITK chip developments forward.

Procurement and transport

Logistics suffered in many areas from COVID. Delays in production, unavailability of products and increases in cost were observed in various project areas. Of particular concern are the procurements of ASICs, EoS cards, carbon foam and pre-preg, for which the situation will not improve until the end of year. The transport logistics arising from ITK distributed production model are very sensitive to changes in import/export regulations, involving many national

regulations including changes due to Brexit. The complexity and time needed for procurement, transport logistics and legislation are (partly) external dependencies that in some cases have been underestimated and deserve more attention in the future.

Site qualification

One of the issues in site qualification is the reviewing process for the required documentation, arising from the large number of documents and the limited number of reviewers. This has the potential to become a bottleneck.

Services

Two minor issues were observed, that will be revisited in the next P2UG. Firstly, it is anticipated that CERN will require CPR (construction production regulation) certification for cables. For type-III cables, no supplier is currently able to deliver with such certification. New suppliers are being searched for and derogation requests are being considered. Secondly, the PP2 design is impacted by the choice of cooling between NOVEC vs. warm CO_2. The PP2 for system test/pre-production is based on NOVEC, while for the production a decision has to be taken and both choices are taken into account for upcoming market surveys/tendering processes. A decision by TC is expected soon.

Recommendations

IS-1: Continue implementing and deepening all three proposed schedule slip mitigation actions, while focusing on completing the pre-productions.

IS-2: Prepare a report for the next P2UG on the experience gained from pre-production A and on plans for how to accelerate production.

IS-3: Vigorously follow-up on clearing all shipping routes with national authorities and consider inserting a condition into the site qualifications that requires a demonstration of successful component shipping. Raise awareness across the project on procurement and logistics procedures.

IS-4: In the site qualification process, dedicate appropriate resources to assure that the documentation and reviewing process has no impact on the schedule.

LAr (in-depth review)

The project continues to make progress despite difficulties linked to COVID – in particular, the non-availability of irradiation facilities. At the time of the review, the project has accumulated five to eight months of COVID-related delay with respect to the baseline. Nevertheless, about ten months of float remain with respect to the current LS3 installation schedule.

The management organigram has two positions that are still marked 'TBD': (3.4) Installation & Commissioning and (3.1.5) Front End Cooling. The cooling will be very similar to the existing system but will involve close coordination with the TC.

As already noted in the last P2UG intermediate meeting, following the baseline options chosen, the project succeeded in completing PDRs in December 2020 for the PA/Shaper and ADC. Due to vendor delays and COVID restrictions, the fabrication and testing of the slice test board was significantly delayed, and the PDR is now expected in summer 2021.

Comments on subsystems

Preamp/shaper and ADC

Very good results were obtained for the two designs of the PA/Shaper (LAUROC and ALFE) where essentially all the specifications were met. The decision to use ALFE was made due to the superior

noise performance. The COLUTA chip has been chosen for the ADC. Detailed results were presented to justify these decisions, giving confidence in the collaboration's choices.

Front end board

The FEB prototype has, so far, only been tested with the LAUROC but the collaboration is confident that the ALFE vs LAUROC replacement will have no negative impact on FEB2 development. The LAr group point out that the shaper parts of ALFE/LAUROC are basically identical and have confidence in the simulations already performed - even though the two ASICS are in different technologies (65 nm vs 130 nm). The ALFE PSRR figure is better than LAUROC's and the coherent noise is expected to be superior. This is an important FEB2 performance parameter.

Nevertheless, we consider a FEB2 integrated slice test with ALFE2+COLUTv4 and LSB, LVPS, etc, remains a mandatory step. The effects of the ASIC crisis mean that the ALFE2 will be back from the foundry mid-summer and the COLUTAv4 will follow two months behind. A slice test with FEB2 board can therefore be performed in 2021.

HEC shaper

The HEC version has made very important progress. Good basic results were obtained with the pre-prototype (HPS1) and were followed by a PDR held in December 2020. This made the recommendation to aim for a final HPS2, i.e. with full functionality and meeting all specification characteristics.

The HPS2 design and simulation (circuit level) are completed and submission is planned for May 2021. As for the barrel, an integrated test with the rest of the FE chain will be a further mandatory step.

Calibration pulser

In 2020, the CLAROCv2 chip was extensively tested. Issues were found with rad-hardness for both the DAC and slow-control. However the most important part, the HF-switch, is qualified. The CLAROCv3 (HVCMOS XFAB018 technology) was sent for fabrication in August 2020 and received back in March 2021. It s currently under test.

The whole calibration project is five to six months delayed compared to the baseline but, despite the impact of COVID, has made important progress.

Power supplies

The project aims to have an integrated test with the FEB2 slice test board. Pre-prototype power supplies, including cables and FEB2 power mezzanine test board, have been produced. The testing of individual pieces is impacted by travel restrictions. Tests including full length cables are mandatory.

The highest priority is to perform the radiation tests on the DC/DC converter; especially for the neutron exposure which has never been tested.

Off-detector electronics

The main unknown is the number of FPGAs per board (and the FPGA utilisation) with the associated risk that the power limit of 400W per ATCA slot cannot be met. We note that other subsystems are considering the practical limit to be 350W, so clarification is needed here. Solutions exist (including space for extra ATCA crates) but can have an impact on overall costs.

Conclusions and Recommendations

The LAr group is to be congratulated for the way in which it has successfully maintained progress across the project in the face of severe COVID restrictions. Going forwards, particular challenges

will be new delays imposed by the unavailability of irradiation facilities and the longer than normal lead times from chip foundries and packaging manufacturers.

The year 2021 will be crucial for the project as many of these tests are planned to happen this year and are the key for the project to start moving beyond the design reviews and towards production.

LA-1: The plan for an integrated FEB2 test with the latest ASICs should go ahead this year even if it is with a reduced channel count i.e. 32 instead of the full 128.

LA-2: The currently vacant management positions should be filled as soon as possible.

Muon (in-depth review)

The muon system review proceeded with one plenary and seven drill-down talks. The presentations and materials were clear and well-organized. The committee submitted three questions that were addressed in a follow-up session on the morning after the in-depth session.

There were no P2UG-tracked milestones for Muons completed in the last reporting period (1-Jan-2021 to 31-Mar-2021). A PDR for the RPC Front End ASIC was held in March and was passed with recommendations.

Comments on subsystems

BIS sMDT chambers

sMT production is underway at two sites (MPI Munich, and U. Michigan plus Michigan State) and is proceeding well. Mechanical precision is well within specification and is being monitored at both sites. The production at MPI began in January and the rate is exceeding the baseline goal of two chambers/week. The production in Michigan began in March and is expected to reach a similar rate.

The sMDT construction relies on a complex pattern of component movement among six sites in five countries, including substantial material flow from Protvino. The committee noted that the organization of the project was robust enough to achieve efficient production rates even in COVID conditions. Possible issues with parts shortages were avoided through early procurement and delivery.

BIS MDT Electronics

The ASD chips are being received and tested. Two thousand ASDs were tested manually and gave a yield greater than 90%.

The TDC PRR has been delayed by eleven months because of lack of access to radiation test facilities due to COVID. The facilities are available again, and this is moving forward. Approximately seven months are expected to be recovered with automated tests of TDC with the ASIC testing robot at Fermilab.

Significant progress has been made in integration tests. For the first time, cosmic ray data was taken in the triggerless mode for a MDT detector with a new ASD, new TDC, new mezzanine card, new CSM and a new motherboard.

RPC Detectors and FE Electronics

RPC prototype-1 component production started.

The RPC FE ASIC continues to be a major source of delay for the project, but it is moving forward. A fully functional prototype of the ASIC submitted in April, and this is a major step. It will be important to see the results with this ASIC tested on a chamber, and at the next review the committee would like to see the plans for this test, which is critical in moving forward on the RPC

project. The working schedule is delayed by about one year from the baseline, and a new RPC schedule is being studied for upcoming baseline change, where some schedule contingency can be recovered in the production phase. The committee will need to see the new schedule to understand how work will be organized in the future. While a baseline schedule change is needed to align with reality and restore predictive power, the project should be careful not to introduce excessive technical risks in compressing the production schedule. Also, the baseline schedule change should be coordinated with global ATLAS schedule changes.

RPC Readout and Trigger Electronics

The schedules for the BMO-DCT boards are delayed by about two months, partly due to delays in radiation testing. The low-dropout voltage regulators for the DCT were radiation tested in March 2021, and the prototype design was submitted to the vendor in April 2021. A prototype board is expected in summer 2021.

The PDR for BI-DCT is expected later in 2021. This was delayed by the FE ASIC.

TGC Detectors

TGC EIL4 Prototype-1 was assembled and is being tested. Early test results are promising but require the complete electrical shielding for full tests. The TGC EIL4 schedule has been delayed by about three months due to COVID and another three months due to interference from ongoing NSW production at Weizmann Institute. These delays do not appear to be affecting critical path items.

TGC Trigger and Readout Electronics

TGC trigger and readout electronics are advanced, and no additional delays have accumulated. The PP ASIC production is finished, and the quantity of chips that have passed the QA/QC are already sufficient for the full system. Preproduction tests for the PS board and the JAThub board are expected later this year and next year. The charge monitoring board has passed specification review and the design is underway.

Power Systems

A baseline change was made for the power systems schedule. Market surveys and tenders are now divided into three lots. A prototype phase was included in power systems tender, which saves time in the schedule. The market survey questionnaire has been released and seven responses were received and are being evaluated.

Recommendations

None.

HGTD (in-depth review)

The HGTD project was approved only in September 2020. It was well understood at the time that the schedule had barely any float, but the physics value of detectors using precise timing (in both CMS and ATLAS) was recognised. At present, there is no scope for further optimisation of the schedule as several crucial items are still in the R&D stage. Even though this is well advanced, significant risks and potential for delays remain, which will not diminish much for a couple of years.

There is therefore a significant probability that the system cannot be ready at the required date for installation. Changes to the LS3 schedule would have a potentially major effect on this. However, the collaboration also has a backup plan which would involve staged installation of the two endcaps, which ought to be relatively accessible. As the use of precise timing is a very new technique, it will benefit from commissioning during early HL-LHC operation before the

luminosity reaches its maximum so there is a clear incentive to install one of the detectors, even if the whole system is not ready on day one.

It may be possible to optimise the production schedule in future once the crucial components have been demonstrated and sufficient experience gained. Hence the project needs to be proactive in preparing prototype systems and test setups. The proposed demonstrator will be one of the important steps in this direction.

In the eight months since approval two significant issues have arisen:

- The ALTIROC2 ASIC submission has been delayed by about six months
- Failures of LGAD sensor elements have been observed in beam tests, and are now attributed to knock-on ions and electrical breakdown

The presentations were well prepared with good responses to questions. There are several elements of the detector which can be considered reasonably safe (e.g. HV & LV power and many cables and services) so although they were presented in depth, they are not reported here in detail. Some of them, e.g. DAQ, are based on components that are widely used elsewhere in ATLAS. The schedules of some 'downstream' elements will mostly depend on the availability of the final detector module components - sensor, ASIC, hybridised assembly.

Comments on Subsystems

LGAD sensors

Since the project was approved, it has been decided to base the modules on pairs of 15 x 15 pixel sensors, rather than a single 15 x 30 device. This seems wise since it follows advice from sensor manufacturers and will certainly improve the yield. The ALTIROC ASIC is also 15 x 15 so there is not much impact on the module design.

The sensor specifications have been approved in an SPR, and they are agnostic about the manufacturing details, rather defining requirements for physical dimensions, operating voltage and signal size after irradiation, and so on. The PDR has recently been passed but the report is not yet available. One manufacturer has produced full size sensors which meet all requirements and there are several other vendors who have produced prototypes. Investigations are ongoing on the effects of different dopants, particularly C, but mainly to ensure specifications are safely met, not for speculative R&D purposes. Moderately long-term stability tests (obviously short of LHC operation equivalence) have been carried out successfully.

A new concern is the observation of destructive breakdowns in the sensors. It was not clear from the reports how many such events can be expected during HL-LHC operation, which will obviously be location and fluence dependent. What mitigation actions are possible is also not yet fully clear. It is essential to estimate maximum failure rates as soon as possible and to study intensively whether mitigation actions, either in manufacture or operation, can reduce these failures or even prevent them.

ASIC

Evidently the design time needed to complete the ALTIROC2 was greater than foreseen last September. The IDR in January 2021, which included outside experts, added additional suggestions for improvements. The chip is now ready for imminent submission. The chip contains two versions of the amplifier stage, as some unexpected features were observed with the voltage pre-amplifier during tests with a sensor last year. The alternative is a transimpedance input stage, which has a smaller amplitude range of time response. Hence different optimisation is required in each case to maintain the timing resolution. The ALTIROC2 has SEE features included but these have not yet been comprehensively modelled so may need further attention for ALTIROC3.

The manufacture is in TSMC 130 nm, but we were told that the delivery schedule is not affected by the increased foundry demand experienced elsewhere in TSMC. However, there have been pressures in IMEC who organise the submission to TSMC.

Clearly the challenge remains to complete the design of the final ASIC (ALTIROC3), which will be influenced by the results of evaluation of ALTIROC2. Although there seems to be a sizeable pool available for testing, progress will depend on the difficulties encountered. A lot of testing remains, including TID and SEE studies, which will need time. Wafer probing to select working chips will not be possible until the end of 2021 so module assemblies must be made using chips of unknown quality. However, it is vital to press on with the hybridisation, of which there is limited experience and only on smaller (5 x 5) pixel assemblies.

Module assembly

There are several manufacturing sources for this step within or accessible to the collaboration. Modules of 5 x 5 pixels have been successfully produced. The key question is how difficult it will prove to be to produce 15 x 15 pixel units, and then do so on a moderately large scale (22,000 unnits) with high yield. Some features of the design are still open, such as wire bonds vs bumps for power. Sufficient ALTIROC2 wafers will soon be available to begin this step but, even if bonding is successful, it will be necessary to carefully study the electrical performance as soon as possible, so many challenges remain.

Conclusions and Recommendations

Given the tightness of the schedule, preparation for each subsequent stage of testing and production is vital to maintain adequate progress.

HG-1: Estimate maximum failure rates of LGAD sensors as a function of fluence in HL-LHC as soon as possible, and study intensively what mitigation actions, either in manufacture or operation, can reduce these failures or even prevent them.

HG-2: Begin preparations for detail evaluation studies of ASICs. Distribute the necessary testing tasks over the collaboration (e.g. digital and analogue characterisation), and in parallel being the next stage of the design including SEE simulations.

HG-3: Begin preparations for electrical characterisation of the first assembled modules, such that this work can start immediately once they are available.

TDAQ

The TDAQ project has made very encouraging progress since the in-depth review in November 2020. Nevertheless, one observes that the amount of schedule float has shrunk considerably in the meantime.

The general perspective for TDAQ has been clarified significantly due to the decision to use a single hardware-level trigger (L0) and to read out all subdetectors at a rate of 1 MHz. This has various implications in particular on the event filter tracking, which needs a new baseline, as will be discussed in more detail below.

Comments on subsystems

The CTP, MuCTPi, TTC and Global Trigger sub-projects are well on track. L0Calo is delayed due to current resource conflicts with Phase 1 upgrade work, but the project also benefits from the Phase 1 development as various components will be reused, and it still has plenty of float left.

In the L0Muon, the current float is reduced to 50 days, and BCPs are planned. The TGC sector logic is following up on the conditionally passed PDR, and the FDR is planned for Q3/2022. Also, the schedules of the MDT and NSW trigger processors need to be reworked.

There is reduced float in various other subprojects. This is partially artificial in DAQ and EF, as the milestones are deliberately scheduled as late as possible to benefit from the expectable later procurement of the hardware.

For the HTT, it is an important milestone that the AM08 ASIC has been submitted. It is essential to complete the tests this summer to keep this option alive.

Event filter

The event filter tracking needs a new baseline since the recent dropping of the L0/L1 evolution option has changed the situation thoroughly. A decision process has been defined and started since the last review. The study of options involves two task forces:

- Optimized HTT: this task force will study a custom processor with pattern recognition based on AM ASICs, also considering an FPGA-based alternative. This option, originally dictated by latency constraints in the context of the L0/L1 evolution, still has significant technological risks.
- Heterogeneous commodity architecture: this task force will investigate an architecture based on commodity servers equipped with accelerators. The study focuses on the use of a Hough transform on FPGA (TF2). This option could require a significant development project.

Furthermore, a pure software tracking solution, using an EF CPU farm of adequate size, is being studied, which itself could further benefit from GPU technology. The physics and validation studies are being performed under a neutral coordination, and a clear set of criteria for evaluation and comparison have been established. A review group has been created to ensure comparability and obtain a comparative assessment of the results.

These studies for a new EF tracking baseline selection are not part of the original WBS and lead to delays. The EF tracking subproject will clearly need an entirely new resource-loaded schedule, whichever option is chosen.

Recommendations

TD-1: The selection of the EF tracking baseline should place very significant weight on aspects of schedule and technological risks. Also, the availability of adequate expertise should be ensured for each solution.

TD-2: As evolution of computing hardware cost is in general hard to predict, one needs explicit provision for ongoing cost assessments and procurement delays in the updated project plan. The appropriate cost vs risk balance should be considered in the schedule for large hardware procurements for EF and DAQ.

TileCal

The TileCal project continues to make progress across all areas and overall is well on track. COVID has led to a delay across the project of about six months although no WBS item is on the ATLAS critical path.

Since P2UG report, the project has filled the vacant leadership positions in Software and Computing, and all positions across the management organigram are currently filled.

Since December 2020 there have been two reviews completed: PRR of the High Voltage Dividers (conditionally passed); and FDR of the LVBox (conditionally passed). Also, two follow-up reviews were closed off: FDR Front-End cards; and PDR AuxBoard.

Comments on subsystems

Drawer mechanics

The production of Mini-Drawers in Barcelona and Cluj is well under way and on track.

On-detector electronics

HV Active Dividers passed PRR in Jan'21 to allow procurement of parts. Final approval for production requires RETF 2020 radiation qualification. Three PMT test benches are ready, with the PRR planned for Oct'21. Front-End (FENICS) Boards are being assembled in pre-production., with PRR scheduled for Dec'21.

PCBs for the mainboards are arriving this month, burn-in and QC stations are ready, and the PRR is planned for September. Daughterboards are still at the PDR (follow-up) stage due to a re-design and delayed radiation tests, which are now due to happen in June-July. V6 of this board is needed for integrated tests of the electronics chain. FDR scheduled for Dec'21.

Off-Detector Electronics

The carrier board v2 has been delivered. CPM v2 layout is being finalised but the current long lead-time for FPGA orders is expected to push prototype production to September. TDAQi v2 layout is being finalised and prototype production is due to start in August. The FDR for the integrated chain (PPR, comprising CB+CPM+TDAQi), is scheduled for Autumn of this year.

Low Voltage System

The auxiliary Board is at v2 and ready for FDR, and the ELMB-MB is completing radiation tests ready for a PRR in September. Three LV Box prototypes have undergone extensive testing. Currently preparing the FDR follow-up.

LV Brick procurement of parts has started and planning for RETF-2020 radiation tests is underway. The FDR is expected later this year so long as radiation test facilities are available. The delay is not critical to the project.

High Voltage System

This has been through a re-design and delays from COVID restrictions means the FDRs for all four components of the system will happen jointly in November 2021, about six months late. A baseline change to the schedule is being implemented.

Calibration System

A solution for the Cs calibration system based on EMCI/EMP has been chosen. The PDR follow up is planned for November 2021 and has triggered a baseline schedule change with around six months delay to the previous baseline, which is not critical for the project. The CERN groups are studying a new choice of (non-conducting) hydraulic liquid for the movement system which will delay this aspect of the project by a year. Again, this is not critical to the project schedule.

The laser calibration system design (ILANA) has now been finalized, with data sent direct to FELIX at 1MHz. The PDR is planned for June this year.

Conclusions and Recommendations

The Tile group are to be congratulated for the way in which they have successfully managed to maintain progress across the project in the face of severe COVID restrictions. Going forwards, particular challenges will be new delays imposed by the unavailability of irradiation facilities and the longer than normal lead times from chip foundries and packaging manufacturers.

Vertical slice (i.e. integrated) tests are planned throughout the project i.e. LV/HV system, pre-processor, on-detector electronics. Many of these tests are planned to happen this year and are the key for the project to start moving beyond the design reviews and towards production.

TC

TI-1: Ensure the various vertical slice tests mentioned above proceed as fast as possible in order to flag early unknown issues arising from system integration

TI-2: Complete the necessary radiation tests of the daughterboard so it can pass through the PDR stage and relieve a bottleneck with the FE electronics validation

TI-3: Ensure that the Tile project and ATLAS are pushing for a timely outcome from the Cs hydraulic liquid investigation undertaken by the CERN groups.

ITk-Pixel

The ITk-Pixel team provided a comprehensive summary of progress since the last in-depth review in November 2020, with substantial technical progress under the difficult conditions imposed by COVID. Though the negative float to installation is essentially constant, which is a positive outcome given both past history and COVID, it remains incompatible with the overall LHC LS-3 schedule.

From the technical point of view, the Pixel project continues its transition from a design phase through validation to the precipice of pre-production. There are six FDRs between August and November 2021, another five between February and May 2022, and PRRs at a rate of 1.6 per month. Of particular importance will be the Module FDR, which has slipped due to COVID-driven delay, and the On-detector Services and Loaded Local Support FDRs, as these comprise the final critical technical validation before the production phase. The committee eagerly anticipates the technical results which will drive these review processes.

From the schedule point of view, in some sense the situation is positive, as the negative float situation has been held constant with respect to last review, under difficult conditions. However, of the 250 milestones not classified as Completed nor Obsolete, about half have negative distance to critical path, and a third with -3 months or worse. This is despite admirable efforts by the project to work on the schedule including a recent BCP to increase float by parallelizing activities where possible, a bi-weekly a task force to examine the schedule, review planning, and supply chain issues, and the adoption of sophisticated production flow simulation software used successfully elsewhere. It is apparent to all stakeholders that while continual schedule maintenance is vital, there is no possibility to make bring the project as current scoped into compatibility with the current LS-3 schedule.

As a consequence, the Pixel project has started a program to explore scenarios for *phasing*, meaning a piece-wise integration scheme underground rather than full integration before lowering ITk, and *staging*, where the integration and installation of some portions of the full scope are deferred until later in the HL-LHC programme. The goal of this exercise is to determine the boundary conditions for a given scenario in terms of physics degradation, schedule gain, immediate design impact, impact on personnel and budget, and implications for LHC shutdowns beyond LS3. While this study has just started, the project presented a sketch of several scenarios, each with some variants, that they intend to explore on a timescale of completion in mid-summer.

Recommendations

PI-1: Proceed with the plan to examine all the options for resolving the incompatibility between the ITk and current LS3 schedule. We would like to be informed about the progress at an intermediate P2UG meeting, in July.

PI-2: The project must carefully evaluate physics performance of the various options being considered, both in the staging/phasing exercise and in general schedule optimization.

PI-3: We encourage the schedule task force to examine well in advance the administrative issues that can slow down the procurement and the shipping of components between production centers, as part of its mandate, and consider how these can be addressed or engineered out of the plan.