Report of the IV ATLAS Phase-II Upgrade Project Review (P2UG)

ATLAS-P2UG Meeting, 30 Oct., 4-6 Nov. 2020

In-Depth Review: TDAQ, ITk-Pixel, ITk-Common and Tile projects
Regular Review: ITk-Strips, LAr, and Muon projects

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Process

Following the III P2UG review in May, the P2UG met again on Sep. 8 in video-conference with the ATLAS Upgrade Coordinator for the quarterly milestones update. The most significant findings and P2UG comments were reported with a written note to the LHCC Chair.

The preliminary material for the IV P2UG review was then received on Oct. 27th and the review started on Oct. 30th with the first introductory talk by the UC, followed by the TDAQ drill-down session. On Nov. 3rd a plenary session with the remaining summary talks took place, while the following day was taken by the ITk-Pixel, ITk-Common/PDB and Tile parallel sessions. On Nov. 5th, the P2UG met with ATLAS management and, after receiving feedback in written form on several questions, convened in an executive session for the rest of the day. The preliminary feedback from the review was presented to ATLAS in the closeout session on Nov. 6.
All meetings were held in the afternoon, via videoconference, due to COVID-19 travel restrictions. As usual, ATLAS made available in advance a snapshot of milestones, taken on October 1st, the summary report of the last internal reviews and the recently updated Risk Register files. After examining the documentation, the P2UG sent in

advance to ATLAS a list of requests for clarifications that were provided during the review.

The P2UG was pleased to see that very important steps forward have been reported in this review. We would like to congratulate ATLAS especially:

- *for having concluded the long, demanding and difficult process of converging toward a decision on the implementation of the L0/L1 trigger and RR, that was well organized and timely executed;*
- *for all the effort invested to improve and consolidate the schedule;*
- *for trying to recover part of the accumulated delays in particular in the ITk project.*

We also commend the UC and the projects for the high quality of the material presented and the highly appreciated rapid feedback to our requests.

General comments on the schedule

The P2UG believes that the improved schedule has now become a tool that can be effectively used to manage the project and that related metrics, like the d.f.c.p., seem to be finally under control.

On the other hand, despite all the efforts to recover delays and securing contingencies, we have had a confirmation, supported by the impressive amount of work presented during the review, that the ITk schedule remains largely incompatible with the current LS3 end date. This as an issue that will have to be resolved next year, when also the revised HL-LHC schedule becomes available. We have been informed that an open discussion with the experiments on the current status of the P2 projects vs. the LS3 schedule will start at the next LHCC.

Recommendation:

GE-1) We invite the ITk project to work with ATLAS and CERN management to explore options for resolving the tension between LS3 and ITk readiness on the time scale of next Nov. P2UG review.

Milestones

The status of milestones completion, updated on Oct. 1st, and the progress in the last reporting period (Jul. 1st - Sep. 31th 2020) are summarized in the following table. The global fraction of milestones achieved in the reporting period (26.1%) is in line with to the values obtained in the previous two quarters, also affected by COVID related delays (17.9%, 26.2%), and remains still significantly lower than the value registered in the last quarter of 2019 (61%).

Project	*All*			*Expected to be completed in the reporting period (Jul.1st- Sep. 31th)*		
	Tracked by P2UG	*Completed*	*Completed over Tracked*	*Tracked by P2UG*	*Completed*	*Completed over Tracked*
TDAQ	163	10	6.1%	5	3	60.0%
ITk-Pixel	340	10	2.9%	6	0	0.0%
ITk-Strips	210	20	9.5%	9	1	11.0%
ITk-Common/DB	66	17	25.8%	8	3	37.5%
LAr	86	15	17.4%	2	0	0.0%
Tile	112	31	27.7%	5	2	40.0%
Muon	142	33	23.2%	11	3	27.3%
TOTAL	1119	136	12.2%	46	12	26.1%

Projects in-depth review

TDAQ

The in-depth review of the TDAQ project proceeded with one plenary and seven parallel sessions. The presentations and materials were well structured, detailed and informative. Given the clarity of the reports, the reviewers saw no need for follow-up questions during the meeting.

General Observations and Comments

The project has generally progressed very well since the last P2UG review. The baseline change process has been completed, resulting in the absorption of most COVID-19 related effects to date, and increases in the float in most areas. During this year important strategic decisions were taken by the TDAQ project and by the ATLAS collaboration as a whole: as a result there will be no regional readout implemented in the pixel tracker, significantly reducing the complexity of the readout, and the trigger architecture will remain as envisagee in the baseline design, with a single hardware level (L0), without splitting into L0/L1 levels. As a consequence, there is now a clear planning basis for virtually all TDAQ components. Everything will be based on a 1 MHz

output rate; there is no further need to maintain "hooks" to support the L0/L1 evolution, all of which is facilitating the development for the components. The COVID-19 impacts are understood and so far under control. Overall, there is currently about one year of slack in the schedule for the tightest paths, which seems appropriate.

Sub-project specific Observations and Comments

There is evidently smooth progress in the L0 trigger area. The muon sector logic hardware PDR was conditionally passed, and the PDR for the MDT trigger processor was recently held. In L0Calo, most of the activities currently focus on completion of the Run 3 components, which will, however, be largely reused for Phase-II. The layout of the central trigger has been greatly simplified by the recent trigger architecture decision. TTC and MUCTPI have adjusted their schedules with the baseline change request and are proceeding well. The Global Common Module and Production Firmware Deployment Module prototypes of the global trigger have been submitted for fabrication.

The power consumption of the Global Common Module was found to exceed the permitted limits, but there is hope this can be mitigated by switching to another FPGA, among other measures. Should this not resolve the issue, a possible means of mitigation would be a reduction of the logic speed, which, however, would reduce the capabilities of the trigger.

In the Event Filter, a crucial remaining design choice is the EF tracking technology. The HTT is still the baseline, with an FPGA-based option being investigated mainly as a fallback in case the AM-based solution should fail. The solution based on commodity farm nodes, which was originally only envisaged for a pileup of up to 140 interactions, is now considered with a scope extended to a pileup of up to 200. There are significant cost reductions due to a lowered CHF/HS06 cost relation on the market. The impact of GPUs and accelerators, which could further improve the cost efficiency, is under study.

For the HTT, the development of the AM ASIC is on the critical path. The FDR for the AM08 chip was recently passed with a delay of about 10 months. As we write, the submission is pending in the next days. The still higher complexity of the AM09 chip was noted as a concern at the FDR review, as well as the need for a significant strengthening of the devloping team, which is currently in progress. The FPGA-based alternative effort also appears understaffed, and studies have already revealed that a significantly higher cost is expected compared to the AM chip solution.

In the DAQ area the development is well on track. Important progress has been achieved with software development, in particular concerning FELIX and dataflow. The network project currently focuses on the tracking of technology to maximize the benefit from its development. The online software project has achieved its first milestone and is proceeding well.

Recommendations

TD-1) For the HTT, the timely characterization of the AM08 chip by next summer is crucial since there is clearly still high risk involved in this project.

TD-2) The evaluation of commodity server-based EF tracking, taking every possible advantage of GPUs and accelerators, should be pursued with high priority.

TD-3) ATLAS should once again design and execute a transparent decision process between the different EF tracking solutions. This involves the adequate definitions of the performance metrics, the decision flow and a clear timeline. The P2UG would appreciate an update at the intermediate meeting in February 2021.

Tile

The Tile project gave a very comprehensive overview of the current status. Good progress was reported across the board, although it was clear that the effects of the COVID-pandemic are now starting to have a real impact on schedules.

General Observations:

Since the last P2UG meeting, the Tile project has undergone a change of project leader: Pavel Starovoitov has taken over from Christophe Clement. Fabrizio Scuri remains as the Deputy Project Leader and a new lead for the Software and Performance working group is being sought.

Baseline change proposals have recently been approved in the following areas:

- PMT procurement and PMT characterization test stands: the delivery schedule now matches what HPK can comfortably achieve and still retains a year of slack before installation. The PRR has shifted from August ’21 to October ’21.
- The procurement of long optical fibres w slighty ill now be made as a common order with the LAr project and will be ready in July ’24, approximately 1.5 years before the installation deadline.
- The Prometeo teststand, needed to test the front-end electronics chain, has had its FDR moved back from Feb. ’21 to Sep. ’21, but schedule changes have been introduced to maintain the PRR date of Oct. ’22.

Detailed Observations – Technical areas

Mini-Drawer Mechanics/Tools/Services:

- The first batch of 20 super-drawers are complete (from ITIM, Cluj Napoca). The first batch from IFAE (Barcelona) has been delayed by procurement issues but is expected in Feb. ’21.
- Tooling has already passed PRR and the Services have a PRR due in Dec. ’20.

PMTs/Active Dividers:

- Indentical QA test-stands have been set up in Pisa/Bratislava/CERN.
- No PDR/FDR is formally required but there will be a PRR after completion of long-term stress tests of new PMT prototypes and pre-production active dividers (currently set for Sep. '21). The project is running slightly ahead of schedule.

FENICS and Main Board: front-end signal shaping, integration and digitising:

- FENICS: a manufacturer for production has been selected, the burn-in station is being finalised and excellent noise/linearity has been demonstrated. A pre-production run is scheduled for Dec. 2020 with a PRR set for Q4 of 2021.
- Main Board: PRR is set for Q2 2021, which requires the completion of a vertical slice test. This is currently being held up waiting for the delivery of v6 of the Daughter Board.

Daughter Board; control and readout interface for the front-end electronics:

- The v6 design is almost complete, which addresses the issues seen with the previous version e.g. FPGA latch-ups after irradiation.
- These issues have resulted in delays, but the project is now on track for FDR in 2021. The NEIL and TID testing of v6 components remains to be completed. V6 boards are expected to be available in Q1 2021 for the front-end vertical slice tests.

Off-Detector Electronics; data processing via the CPMs and interface to the trigger/FELIX via the TDAQi board:

- The fast link between CPM and TDAQi (10Gbps) has now been demonstrated (made possible by changing to Megtron 6 dielectric material on the Carrier Board).
- The FDR for the full chain (Carrier Board + CPM + TDAQi) is planned for July 2021.

Low Voltage Distribution:

- The LV brick FDR was passed in Oct. 2020 (NIEL tests of the op. Amplifier must still be verified).
- The LV box design has addressed the recommendations from the PDR and the FDR is set for the end of 2020.
- The Services design is complete (the Aux Board). The PDR was passed with follow-up. The Bulk 200V supplies are commercial units and will only require a PRR.

High Voltage Distribution:

- The project has suffered delays mainly due to the design of the HV supply board taking longer than expected. The PDR is now scheduled to happen by Q4 2020.
- A HV vertical slice test is required for the FDRs of all elements of the HV chain (HVBus, HVremote, HV supplies, Cables) and is now scheduled for the end of this year (without the HV crate, which is progressing but will not be ready in time.)

Calibration; Cs system (tiles)/Laser system (PMT's)/charge injection:

- Most systems are still in the design phase with PDR and FDR milestones over the next 2 years.
- The Cs system has new electronics and there is an update to the hydraulic source distribution system.
- The Laser system has a new control interface (ILANA) to comply with the upgrade TDAQ.

- There is a dependence on the new Embedded Monitoring and Control Interface (EMCI, the replacement for ELMB++). EMCI prototypes are expected for Jan. '21 which should allow a PDR for the electronics around Spring '21. The PRR date is unchanged and expected in 2022.
- A new calibration interface is being developed in firmware which will supervise calibration requests to use the accelerator empty bunches and forward these onto the trigger.

Assembly and Integration:

- A full plan for drawer assembly and installation exists that fits the current LS3 master schedule. Manpower and a timetable for all stages of work have been calculated.
- Bat. 175 and 171 at CERN have been studied and found to be suitable for all storage, assembly and testing needs of the project.

Comments:

- The TileCal project is to be commended on the very real progress that has been made over the last period and on the generally healthy state of the schedule across the board. There are no areas giving significant cause for concern and there is a high level of confidence that the project will be delivered both within spec. and within even the most aggressive timeline scenarios for LS3. Significant COVID delays on top of those already encountered could however change this picture and must continue to be closely monitored.
- The relatively small float (150 days) for the electronics and hydraulics of the Cs calibration system, is considered to be rather conservative, since it is referenced to the very start of LS3 and will remain so until the installation schedule for LS3 is established.
- Integration of the Cs system with EMCI-EMP will allow simplified Cs control boards which are expected to be radiation hard. Good links with the EMCI development team are reported and will remain important going forwards. We note that this aspect of the project represents an external dependency, with essentially the same team previously responsible for the ELMB++, in a vital element of the system.
- It should be noted that the assumed activation levels for extracted PMTs come from existing measurements of exposed PMTs extrapolated to the exposure levels of Run 3. We would like to clarify at the first opportunity whether this is sufficient for making PMT handling plans or whether the latter should be based on measurements of real PMT blocks from Run 3.

Recommendations:

TI-1) We would like to see milestones set for the development of the EMCI in the Calibration project (e.g. the EMCI prototypes expected for Q1 of 2021). It is also mandatory to present the feasibility of a backup solution based on the Daughter Board, plus any effects this may have on the schedule etc.

TI-2) We would also like to have clarification of how the new laser control interface (ILANA) and the Tile Calibration Interface are to be incorporated into the review process for the calibration and in the milestones.

TI-3) Early contact should be made with the CERN Radio Protection group to establish what handling arrangements, and working space, must be implemented for the removed PMT blocks.

TI-4) It is suggested that the type of HV connectors and cable be reviewed at this stage and the product search widened. An integrated test to verify the performance and long term quality would be prudent.

ITk-Pixel

The ITk-Pixel team gave a thorough review of progress to date, which includes both substantial technical progress under the difficult conditions imposed by the Pandemic, and important progress in development of their schedule, which is now a useful tool for forecasting progress and investigating potential for accelerating progress. As it remains in tension with the overall LS3 schedule, it is of vital importance to preserve its reliability.

General Observations:

The project presented a complete tour of the scope, covering schedule status, milestones, risks, focus for the coming year, and technical progress. Highlights are:

- completion of 3 PDRs and two FDRs in the last year;
- sensor Market Surveys complete or near completion;
- submission and reception of the first Pixel ASIC specifically customized for ATLAS;
- validation of multiple Hybridization vendors with excellent bump quality;
- further development of workflow through Module Assembly and qualification of Assembly and Testing sites;
- considerable progress developing the new plan for Data Transmission;
- improvement in the Inner System Stave design, to meet Thermal management specification.

In addition, after thorough study and internal deliberation, several important decisions were made recently, allowing for progress on final design in multiple areas:

- the pixel size has been finalized;
- the Layer 0 radius was reduced and various gaps in z were modestly increased for clearances;
- the possibility to read out a portion of the Pixel detector at 4 MHz rather than 1 MHz has been dropped;
- further development of the “Regional Readout” functionality envisioned for the final Pixel Chip has been abandoned.

Despite the progress mentioned above, the project still faces schedule challenges, both in the near term in and the long term. The project has suffered schedule slippage of the

order of 3 months in near term milestones, chiefly due to the COVID pandemic, which propagates into the forecasted execution dates through quarterly updates (“statusing”).

Since the last in-depth P2UG review, the project has invested heavily in reworking their schedule to make it a reliable planning tool, allowing credible forecasts and schedule optimization exercises. This is demonstrated by their analysis of the critical path, which shows a negative float of 118 days between the ‘ITk Pixel Outer System ready for insertion’ and ‘TC Outer System need-by date’. With a solid command of the schedule tool, the project has performed some mitigations already, and proposed several more, which they are encouraged to pursue. However, exacerbated by the COVID scenario, there are now multiple near-critical path sequences such that more schedule manipulation to deliver the current scope is very unlikely to resolve the incompatibility with LS3.

Detailed Observations – Technical areas

- 2.1.1 Sensors: The sensors are aiming for Pre-production in 2021. The Planar FDR Sept 2020 was passed, and Planar Market Survey (MS) ongoing, and the 3D MS complete, tender in progress. QC plans for both are on track.
- 2.1.2 FE ASIC: The ITkPixV1 submission was delayed by front-end selection and high resource demand verification, and upon testing revealed a bug in ToT memory latch design, which connects power to ground for non-0 setting, causing large current draw. This design feature was not utilized in RD53A, and was overlooked in validation, due to a combination of miscommunication during personnel turnover and lack of sensitivity in older verification tools.

  To mitigate this issue, the project executed a fast re-submission with metal layer patch to make V1_1 ASICs, with the first batch using modified metal layer processing on 4 wafers already at TSMC for early samples, and pre-production batch being ordered. This version will only have binary readout, and cannot be used in serial power chains, but other functionality can be checked and so far it looks like, but for the flaw, it could have met production specs. Full fix will be verified with CMS CROC submission, so it does not affect V2 submission date. Wafer probing QC for the ASIC is in development, with a prototype probe card produced.
- 2.1.3 Modules This WBS consists of Hybridization (bump bonding) and testing, and Assembly with PCB and subsequent testing. The Hybridization MS is expected to complete in Dec. 2020, and the FDR is scheduled on Nov. 25, 2020. This FDR is based on dual-chip modules, most of which already delivered, and currently the testing is ongoing with satisfactory results so far. Module Assembly is moving from dual-chip to RD53A now, and will incorporate ITkPixV1_1 for FDR in June 2021, with pre-production in latter half of 2021 to demonstrate procedure and throughput. There are a large number of assembly and testing sites, but a clearly factorized flow of components to assembly and testing locations. Many sites are undergoing validation now, with the use of

"digital quads" to validate testing sites. The Module assembly group is still in final assessment stage on several topics affecting:

- Robustness: bump stress, radiation hardness, encapsulation;
- Materials: adhesive between module and PCB, parylene coating;
- Procedure: Glue pattern.

- 2.1.4 On-detector services: The scope is module pigtails, PP0/EoS panels, power connection to PP1, and MOPS, the monitoring ASIC. Currently prototype fabrications are being completed to feed System tests of loaded Local Supports in 2021, with the FDR in Feb 22. This is on the critical path, but many near-critical items anyway, so no big gains to make in speeding this up. There are the typical missed milestones in 2020 due to pandemic, but progress is reasonable. The main remaining decisions are in design, signal density and cable mass vs. noise/crosstalk. The various components are somewhere between existing conceptual design to prototype under test.

- 2.1.5 Local Supports: The scope is the mechanical support and cooling for modules, and Local Support loading/testing. Here again ther eare milestone delays, due to the pandemic, and upstream dependencies, which have delayed final qualification. The focus of next year is qualification of base Local supports (FDR June 21) and system tests on Loaded Local Supports (FDR Dec. 21). There as still some detailed design choices to be finalized, such as adhesives for module loading, coating of LS, wire-bond protection during pig-tail routing. RD53A Quad module loading and system tests will inform these decisions.

  In this sector, complexity is significantly reduced by 4->1 MHz decision, as well as the "distributed PP0", where the patch panel is smeared along longeron. A considerable amount of thermal and mechanical testing shows good results for the bare mechanical supports, and for Loading work procedes for final tooling/procedures development.

- 2.1.8 Off Detector Services: The scope is Electrical Cables and Patch panels to bring services from service cavern to Patch panel 1, Power Supplies, and DCS hardware. They are aiming for Services FDR April 2022,and currently most cables have several vendor design options under consideration, and the panel designs in reasonable shape. There was a need to re-factorize the power supply procurement strategy to alleviate high cost of prototypes with conservative specs, allowing for less performant specs for pre-production testing, which will subsequently inform final production specification.

- 2.1.10 Data Transmission: The scope is the Electrical path from module flex cable through PP0, Optical conversion, to DAQ. The PP0/Elink portion is aiming for an FDR in Q4 2021, and the Optolink for FDR in Feb. 2022. Here as well, there was a large quantity reduction and simplification with 4 MHz -> 1 MHz decision.

  The connection from PP0 to the Optoboard, which houses the GBCR receiver

chip and LpGBTs, is envisioned as a twin-ax cable scheme, with various bundle flavors/terminations scheme for Inner System, Outer System, Endcaps, and with a possible intermediate aggregation for the End Cap to ease cable routing. The Twin-ax went through Fire Retardation verification, more complicated than one might think. The project is working on vendors for twin-ax ribbonization, connectorizing/soldering.

There has been significant progress in this area, with Optoboard/box prototype produced; testing functionality and robustness shows good results. Tests with protoype parts show BER < 0.2×10^{-12} to optobox, and the GBCR chip functions properly. However, several things still need attention: the impact of Twin-ax termination on signal quality is still under study; jitter from the GBCR needs to be understood and tests on radiation robustness/SEE effects need to be performed.

Comments:

We commend the proponents for a well-constructed review, which clearly presented both substantial technical progress, despite the current global health crisis, as well as a candid assessment of challenges ahead and the potential strategies for resolving them. In addition, we applaud the well reasoned and thorough effort to make difficult decisions with full transparency in order to close open avenues which previously hampered progress to final designs.

The story with ITkPixV1 is unfortunate, although the team has done well to recover. Given the proliferation of ASIC development across the LHC Upgrade, it would be beneficial to formally propagate lessons learned from ITkV1 experience.

The review committee concurs with the decision of the project to focus on the near term goal of getting through the "Year of Final Design Reviews", assuming that the tension between readiness and LS3 will be addressed, as the global pandemic unfolds and CERN directs its attention to the impacts on the LS3 schedule. *It should be noted however that an indeterminate endgame makes the baseline uncertain, and may induce further delay due to funding agency authorizations.*

There are 13 Final Design Reviews between Nov 2020 and March 2022, 7 of which are scheduled before the next P2UG meeting, thus on many fronts the critical activity is to finalize all remaining design choices and complete the validation. Of particular concern are:

- Validating as much as possible the ASIC design based on ITkPixV1.1 so that there is high confidence a chip submission beyond ITkPixV2 will not be necessary
- Completing the twin-ax termination decision, with consideration for the ramifications if rework at PP0 is required
- Propagation of functional modules (RD53A, ITkPixV1.1) through to Loaded Local Services and testing full functionality

Recommendations:

PI-1) Complete the work on improving the schedule, started several months ago, and the ongoing effort to explore residual possibilities to reduce the final mismatch with LS3 schedule.

We would appreciate to have an update on this at the next P2UG Interm. meeting.

ITk-Common/DB

The ITk-common project has seen significant progress in all areas since the last in-depth review in November 2019. Until the end of Q3-2020, 17, out of the 21 P2UG milestones, have been completed (i.e. 81%) with four open milestones due by the end of 2020. The project is generally well on track in the preparation of common items. Nevertheless, major schedule concerns are evident and arise from delays inherited from other subsystems.

The awaited inter-linking of the five ITk L2 subsystem schedules (Strip, Pixel, Common Electronics, Common Mechanics, and Database) has been implemented via a configuration file. This consolidates the schedule robustness and reliability and represents a significant help in tracking the overall ITk project. Further improvements in the schedule handling are expected within the coming 3 months. In particular, the calculation of distance from critical path of common items, which presently inherits slack from the Pixel and Strip schedules, will be corrected. Together with the outstanding baselining of some common mechanics subprojects and the addition of further milestones, a further improved technical implementation and handling of the schedule is expected.

ITk-Common Mechanics (CM)

ITk CM is well advanced and about to freeze the designs and material budgets for the common mechanics deliverables and enter the project phase, in which significant changes can only be implemented on the basis of Engineering Change Requests. It is noted that the decision on the trigger has largely relaxed the service constraints with positive impact on CM resources.

CM includes the ITk surface integration and commissioning, which made good progress and remains on schedule towards readiness for integration. The SR1 layout definition and the pixel and strip integration steps were agreed, documented and supported by detailed 3D modelling. The use of a DEMO cooling plant with the Lukasz cooling system remaining as a backup was agreed with the cooling team, and a need date for the cooling to be ready for the integration facility was fixed.

Comments:

- The P2UG welcomes the formation of the "CO_2 Oversight Board" which closely follows the R744 primary cooling plant project and reports directly to LHCC, LETEM and CERN Directorate. Within the P2UG review, concerns based on the recent experience with the installations of the LHCb CO_2 cooling system have

been raised that the estimated resources and installation times might be underestimated. These concerns shall be carefully evaluated.

- The previously reported manpower shortage in the cooling project has been mitigated, while care has to be taken to maintain the level of person power and expertise in the cooling team throughout the upgrade project. In particular, for new commitments, like the potential replacement of the present C_6F_{14} cooling for cables and optoboxes at PP2 with a «Warm CO_2 cooling» in view of CERNs Green technology environment policy, care must be taken to not compromise resources dedicated to the ITk common cooling project.

ITk-Common Electronics (CE)

The Environmental Monitoring is largely on track, with the radiation-monitoring project being even ahead of schedule. A new group joined the project to produce a sniffer system to complement the fibre optic sensors for humidity measurements. The temperature sensors are needed at an earlier stage for the strip system test in July 2021. The PDR was passed with several recommendations in July 2020 and the project is aiming for an FDR in January 2021. COVID related delays and delays in radiation testing provide a concern that not all foreseen qualifications will have been achieved at the time of the FDR. The subject will be revisited in the May review.

Within the Interlock project, two prototype crates have been built. The FDR in July 2020 was only conditionally passed with several follow-up actions. The problems are being addressed and do not pose a concern at this point in time, as there is sufficient contingency in the schedule. The Grounding and Shielding (G&S) core team consists of 3 persons that closely follow all PDRs and FDRs of ITk components for potential G&S issues. Testing procedures for production and installation sites are in preparation.

The project on the Luminosity and Beam Protection device (BCM') has made good progress, but remains an ambitious and very complex detector project by itself. It carries all interfaces of the larger ITk subsystems, has dependencies on external deliverables (picoTDC, lpGbt, bPOL,..) and ongoing sensors, FE ASIC and readout-chain developments with decision points ahead. The ready for installation date of May 2023 appears very challenging to the P2UG, especially in view of the limited resources of the BCM' project.

Recommendation

CO-1) We invite the BCM' project to address the critical aspects presented in the review and to secure the resources needed to match the installation schedule. We will ask for an update of this effort in the P2UG May review next year. ITk is also asked to evaluate the impact of not matching the presently foreseen installation date.

ITk-Common Production Database

The project has made good progress and is now linked with the FDR and PRR milestones for the ITk subsystem components going into the database.

Other Projects

ITk-Strips

The ITk-Strips team presented a summary of their activities since the in-depth P2UG review of the project in May.

Observations

The ITk-Strips project has had several important advancements in this period. These include:

- completion of the sensor pre-production;
- successful SEE testing of the pre-production ABCStar ASIC;
- completion of the FDR for the AMACStar ASIC;
- identification of the source of the Long Stave (LS) noise at low temperatures, clearing the barrel bus cable pre-production; cold noise studies of the Short Staves (SS) and endcap petals are on-going;
- launched endcap petal assembly IT;
- global mechanics entering production.

The project has seen significant delays due to COVID. These include:

- slower procurement activities and longer market surveys;
- slower laboratory turn-on and reduced staff availability;
- impact on internal communication and site qualification due to lack of travel.

The delays in various sub-systems, from 3 to 5 months, has reduced their float from 111 days to 18 days. The project team is preparing for a BCP that will include adjustments for various schedule changes.

Comments

The project has advanced on several fronts since May, despite the extremely difficult circumstances due to COVID. Many aspects of the project have entered pre-production stage. The team should be commended for their effort.

A major part of the delays is due to COVID. However, significant delays have also resulted from the mitigation effort on the readout ASICs SEE issues. The HCCStar is still in design for SEE mitigation, including increased triplication. Despite the need for extra space in the chip, all variants of the HCCStar design remain compatible with dual L0/L1 trigger. The HCCstar FDR is scheduled for December 2, but it is not certain that the design will be completed by then. The completion of this effort and the related tests

remain among the main drivers of the project schedule. They plan to combine the submission of AMACStar and HCCStar.

Owing to the improved schedule for lpGBT, they no longer plan on using pre-production chips for temporary EoS. The availability of the CERN ECE chips remains a key schedule driver, therefore the improved lpGBT schedule represents a major step forward.

Recommendations:

ST-1) Regarding the combined submission of HCCStar and AMACStar chips, the review committee finds the argument of cost-saving from a combined submission vs time-saved from an early AMACStar stand-alone submission reasonable. However, we are concerned that the time for mitigating potential SEE issues in any of the two chips has very large uncertainties. The committee, therefore, recommends that in the event of a significant further delay in the HCCStar design completion, consideration be given to a separate AMACStar submission.

LAr

Observations

Despite COVID it seems that there has been good steady progress in several areas. Nevertheless a number of milestones have been shifted to December 2020, as consequences of tests not completed.

Two important PDRs are planned before the end this year.: PA/SH and ADC (including choice of the ADC option).

The project made a BCP (Baseline Change Proposal) in September to include changes in the LS3 schedule, mainly to accommodate:

- for the Calibration Board, the addition of a TSMC 130 nm CMOS DAC chip development, as it was realized that the DAC part of the CLAROC2 test chip showed too large performance degradation when subjected to the expected HL-LHC TID. The group is confident that two iterations (pre-prototype and prototype) will be sufficient.
- the addition of a Layer Summing Board to take over the trigger path signals from individual calorimeter cells that need to be summed into “supercells”, as the initially hope to build that functionality into the preamp/shaper chip turned out to be not feasible. This LSB (Layer Summing Board), will be small mezzanine board on top of the FEB2.(Front End Board 2) and the LSB technical details and planning will have a P2UG review in May 2021.

Comments

From the schedule point of view there is still ample float to accommodate these changes. Identified teams will take responsibility for the development of the Layer Sum Boards and for the two ASICs needed on the calibration board.

The FEB2 slice test incorporating the FEC LVPS (Front End Crate Low Voltage Power Supply) continues to represent a major milestone of the project.

Muon

Observations and Comments

In the Muon system, three major PDRs have been completed in the last six months: RPC gas gap and readout panel, EIL4 TGC, and the RPC DCT board.

The PRR for BIS1-6 of the MDT project has been completed. The preparation for sMDT chamber production has made good progress and production is ready to begin. The module 0 was completed at MPI and production will commence at this site in few weeks with a planned rate of 2 chambers/day. A second site (University of Michigan and Michigan State University) will begin the production of 2 chambers/day in December 2020.

MDT electronic production is proceeding very well. The ASD ASIC PRR passed in April, the full production has been completed and now they are waiting for packaged chips. The TDC ASI test has been postponed to Q1 2021 due to COVID-19.

A pre-prototype of the RPC FE ASIC was submitted in September to test the analog part. The submission of the full prototype has been delayed by an additional four months, and is now foreseen for January 2021.

In spite of COVID, progress has been made in almost all areas. Nonetheless, about half of the projects have a distance from critical path of less than one calendar year. The effect of delays on schedule contingency will need to be followed closely.

The FE ASIC for RPC continues to be a concern in term of manpower and schedule.

The schedule for the Power system is very close to the critical path (18 days) and so a reworked is needed.

No news has been reported about the LV distribution for RPC FE. We would like to receive an update at the next review.

It seems possible that ATLAS Muon will have to operate a HV system with a mixture of different types of hardware. This will require availability of additional efforts and planning on firmware and high-level controls expertise.

Recommendations:

MU-1) We would like to have an update about the status of the RPC FE ASIC at the February P2UG interim meeting. If the prototype is not submitted in January, an evaluation of the performance degradation and schedule impact of possible alternative options should also be presented.

MU-2) For the May review, we would like to see a schedule for the power systems that provides a realistic evaluation of the schedule contingency.