Report of the ATLAS Phase-II Upgrade Project Review (P2UG)

First ATLAS-P2UG Meeting, 7-8 May 2019

In-Depth Review: ITk-Strip, Muon and LAr projects

Regular Review: ITk-Pixel, ITk-Common, TDAQ and Tile projects

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The agenda and presentations can be found here:
https://indico.cern.ch/event/815877/

Process

The yearly cycle of the ATLAS P2UG reviews currently consists of two two-day-long review meetings held at CERN and two status update Vidyo meetings, distributed over the year and synchronized with LHCC meetings. In the reviews at CERN, half of the projects are reviewed in-depth while the others present a general status update.
It was decided with ATLAS to schedule the in-depth reviews of the Muon, LAr and ITk-Strip projects on May 7-8, 2019 and the remaining ones on November 5-6, 2019. The intermediate status update meeting in 2019 will take place on the 4th of September.

In preparation of the first review, the panel received from ATLAS (at the beginning of March 2019) a preliminary list of milestones, to be tracked by the P2UG, for the Muon, LAr and ITk-Strip projects. The P2UG panel checked their structure and level of granularity and after an iteration and a Vidyo meeting with ATLAS held on April 1, followed by the submission of a second version of the LAr milestones, approved the format of the milestones.
On April 23rd, the panel received from ATLAS, for the projects subject to the in-depth review, the agreed set of material to be submitted in advance, consisting of updated versions of the WBS/PBS and of the Risk Register, the list of milestones and a summary of the outcome of the latest project internal reviews. For the remaining projects the milestones and review outcomes were also submitted to the panel just before the review, although for the ITk-Pixel the list was very preliminary and not complete.

On May 7 the P2UG review took place at CERN with four-hour long plenary sessions, followed by three breakout sessions in the afternoon and in the following morning session. ATLAS was asked to answer a list of *homework* questions and then invited to participate in a close-out session on May 8 where the preliminary outcome of the review was presented.

General comments

Following the approval of the P2 TDRs, ATLAS has carried out a schedule assessment exercise for all the P2 projects, followed by schedule baseline reviews for most of the projects. In addition, they have been organizing the P2 internal Specification and Preliminary Design as ATLAS wide reviews, with the involvement of strong review panels and with the intent of reducing the risks of major surprises later in the project. Importantly, ATLAS have also synchronized their annual reviews of the P2 projects with the P2UG schedule of in-depth reviews.

We commend ATLAS for their effort in trying to improve the effectiveness of the internal review process for the P2 projects and for the decision of scheduling the Annual Reviews just before our reviews; this choice will certainly be beneficial for the quality and comprehensiveness of the material presented in our review. We have also much appreciated the excellent responses and attitude to address P2UG questions and requests and the clear and comprehensive presentations.

At the time of the May P2UG review, the ITk-Strip, LAr, Tile and Muon projects had implemented all recommendations originated from the schedule baseline reviews, with

final internal schedule verification expected to take place before the end of May for Tile and Muon. However, the review process for the TDAQ and ITk-Pixel projects had not yet converged and follow-up reviews are planned for June or early July.

The P2UG panel has examined the new presented milestones for the projects in in-depth review and, although noticing significant shifts in some cases, it seems that the level of contingency is still acceptable. However the panel is concerned about the still ongoing re-baselining process of the TDAQ and ITk-Pixel projects and is looking forward to its timely conclusion.

Projects in in-depth review

ITk-Strip Project

The re-baselined ITK-Strip schedule has been built "bottom-up" with realistic estimates of durations for both R&D and production, using a sophisticated assembly model. However, the completion of the project within the current plans for LS3 is extremely tight and is very concerning. This will require continual vigilance unless circumstances regarding the entire LHC schedule are altered.

A key driver of the schedule is the rate of delivery of sensors. The schedule assumes an optimistic sensor delivery schedule, although not without historical basis. This should be revisited after the vendor contract is signed.

Observations:

- Most key decisions have been made, although a few important decisions remain to be made, including the decision on pre-irradiation of the ABCstar chip.
  - Upon request, the project team prepared a plan for how they would reach a decision on pre-irradiation of the ABCstar (and possibly the HCCstar) chip. The review panel was satisfied with their approach.
- The progression to production across all areas of the WBS is paced by individual gateway reviews, a Preliminary Design Review, Final Design Review, and Production Readiness Review, and key deliverables to be scrutinized in these reviews. All PDRs are complete, FDRs are ongoing during this and the following year, and the first PRR is next year.
  - The FDR of the ITK common and Strip Global Mechanics that took place in Nov. 2018 did not pass. The project team has been working on responses to the recommendations and is preparing for another FDR in Summer 2019.
- The ITK-Strip team has provided a suitable set of milestones for monitoring progress throughout the project. Currently the critical path flows through the fabrication of the ASICs in prototyping/pre-production, and then Module Assembly during production. The last P2UG milestone on critical path is "Barrel ready for installation" on Sept 13, 2024.

Comments:

ATLAS ITK-Strip has made substantial progress in pivoting from R&D towards production. The WBS has been rearranged to facilitate management of production, and the schedule has been substantially developed to encompass more of the details of production, testing, and installation. In addition, many technical achievements have been

made, culminating in the production of a fully loaded double-sided stave. Overall progress is excellent and many technical issues have been resolved.

ITk-Strip sub-projects

Observations:

- ITK Strips maintains a Risk Register. Currently there are 63 threats, 13 High, 35 Medium, and 15 Low rank. There are also 6 opportunities, 4 High and 2 Medium. Of particular concern are:
  - HPK is the sole vendor for the sensors, with similar commitments for CMS; hence sensor production throughput is one of the biggest risks to the schedule. Few handles currently exist in mitigating this risks.
  - The module and EOS chipsets are powered with the BIPOL12 DC-to-DC converter chip. The input voltage to the chip is now reduced to 11 V, hence removing most of the headroom.

Comment:

SEU rate of the ABCstar and HCCstar chips are not yet determined. If the results anticipated from recent radiation studies show high SEU rates, any major required revisions of the designs can impact the schedule and, potentially, the cost.

Recommendation for the November P2UG meeting:

The panel requested that a presentation be given at the next meeting on grounding and shielding the ITK elements, detailing the local and global grounds in the system.

Muon Project

Observations and comments:

The Muon project is well defined and organized. Schedules and milestones are realistic, including some contingency in most cases. The manpower seems also to be under control. The delay of installation of the Phase 1 New Small Wheels (NSW) has added some schedule uncertainty and additional resource requirements for the ATLAS Muon community. The Phase 2 project is making adjustments to avoid negative interference, but possible resource conflicts with NSW have to be monitored.

Muon sub-projects

Comments

- RPC :
  - the project still has few important decisions to be taken:
    - eta-eta vs. eta-phi on RPC readout;
    - material for RPC strip panel;
    - TDC integration in the front-end electronic.
  - The path to settle the last open technical aspects is defined and clear; the final RPC detector configuration should be finalized as soon as possible.
  - Mechanical production schedule is very long but could be improved.

- Upgrades will change the power/heat load (up in some cases, down in others) and in some places the temperature could exceed the present limit of 28 ^{o}C. A comprehensive look at power and cooling would be useful.
- TGC and more:
  - The Patch-Panel ASIC run has been performed well ahead of schedule.
  - The Service Patch-Panel Board is to rely on an SD card for rebooting. There is the need to minimize chances of corrupted SD card or to implement a recovery scheme.
  - The Triplet EIL4 design is still to be completed. Mechanics and possible cross-talk will be studied in the next months. To be reviewed in the next P2UG meeting.

Recommendations:

- The MDT/RPC combined test at CERN should be better defined and the time needed quantified. Any possible induced noise between the two detectors should be studied in advance of installation, using the final electronic chain up to the trigger.
- ATLAS should consider building at least 1 spare for each of the 7 types of RPC to be used in case of problems during the installation phase.

LAr Project

Observations and comments

Since last year's UGC review, the LAr project has matured with intense R&D activities that have made it possible to pass the dedicated "Specifications Reviews" early this year and to develop a well detailed technical plan and an improved organization of the management team.

The corresponding re-baselined schedule is now defined, keeping a 1-year float, and is deeply detailed.

In those cases where multiple options are still open, the decision will be taken at the time of the Preliminary Design Review (PDR), e.g. for the PreAmpl + Shaper and the ADC.

The critical paths, FE ASICs and FEB2 board, are well understood as are the remaining risks.

LAr sub-projects

Observations and comments:

PreAmpl + Shaper

Both LAUROC1 and ALFEv0 ASICs gave encouraging results, the PDR is now shifted to Q2 2020 at the time of LAUROC3 submission. Since the last review, progress has been made on the HEC version with the addition of extra manpower (TRIUMF) to the project in coordination with the other teams.

Front-End Board (FEB2)

An incremental approach has been adopted that looks well suited for the accommodation of ASICs (PA+Shaper and ADC) development steps. A readout system (à la phase I) needs to be setup independently from the LASP development.

Calibration Board

There has been good progress on HF-Switch. The decision to develop the DAC in the same technology (HV-CMOS XFAB018) and integrate it with the HF-Switch is good, even if it adds some delay (keeping the overall schedule). Backup in TSMC 130nm technology is foreseen.

ADC

Progress have been made on the COTULAV2 (custom ASIC) and also on the IP ASIC solution via contract/collaboration with the S3 company.

The PDR is scheduled for the end of 2019 to coincide with the results of COTULAV3 and the IP-version.

If the IP version is chosen for any reason, the ancillary digital logic which has to be added will have to be developed.

At the time of the PDR the COTS option could be ruled out.

Liquid Argon Signal Processor (LASP) board

Since the TDR, it was decided to split the board in two and to have an independent board (LATS) dedicated to Timing only. We consider this a sound approach.

The LASP specifications have still to be detailed and refined to match the requirements of the front-end boards and of the readout and trigger boards.

One important open issue is the power consumption of the baord which amounts to 410W for the main blade and 50W for the SRTM. Although the team is well aware of the issue, the backup solution has not been selected yet from the available options and validated.

HEC Low Voltage Power System

The main issue for HEC seems to be the availability of ELMB2. This could have planning implications and needs to be careful tracked. In addition, the trade-off between using ELMB2, with periodical replacements, vs. developing the ELMB++ (radhard version) board is still under discussion and a decision should be made in a timely way.

Recommendation*:*

Try to take the opportunity of the already planned slice test to perform a FEB2 radiation test (with protons) to understand and verify possible SEE/SEU issues, even if the used technology is qualified radhard.

Other Projects

ITK-Pixel Project

Observations:

A summary of the current plan for ATLAS pixels was presented, while the detailed review is for the Fall P2UG meeting. Several open-ended issues (inner radius, 25x100 μm, services design, regional readout, PPo design) were discussed. At this point there is an estimated delay of 6-8 months.

Comments:

The schedule delay, and continued need for R&D and in some cases simulation to inform decisions, are very concerning.

Recommendation:

ATLAS should prepare a preview of the November Detailed Review for the September 4 ATLAS P2UG vidyo meeting, presenting the baselined schedule and an update on all the open issues, which include a discussion of timescales for decisions and quantified impacts of the options under consideration. The updated Gantt chart and list of milestones should be communicated to the P2UG as soon as available, and no later than two weeks before the meeting.

ITk-Common Project

Observations:

- Baseline schedule reviews are still ahead: Common Electronics & Production Database scheduled for May 2019 and Common Mechanics for June 2019. At the time of the P2UG review no milestones were available for WBS 2.3 (Common Mechanics) [There are 25 milestones for 2.4 (Common Electronics), and 3 milestones for2.5.1 (Production Database).]
- The FDR of the ITk Outer Cylinder (2.3.3.) was not passed on Nov.18. The revision of the FDR is foreseen for summer 2019. Passing the FDR revision is essential to arrive to the PRR within schedule.

Comments

- The P2UG in-depth review of the common items is scheduled for P2UG Fall meeting.
- ATLAS states that the SR1 integration and installation plans push on the LS3 duration, resulting in realistic concern that ITK will fit within the current time allocation. This statement needs to be followed up (after the baseline schedule review) and substantiated with details to allow the situation to be evaluated in the P2UG Fall meeting.

TDAQ Project

The status was presented in a single report. Additional information was provided in answers to written questions by the reviewers. The MoU is finalized and has been sent to the CERN management. There have been minor changes in the money matrix since February, and overall the coverage has improved.
Currently the number of reportable milestones has increased to about 150, which is still preliminary. The global project organization is being updated; in particular the HTT management is being strengthened.

Observations

The modification of the pixel services design and the resulting increase of material have significant impact on TDAQ. The required stronger data compression may result in increased latency which could be crucial for the L1Track system in the evolution scenario with L0/L1 split hardware trigger levels. A task force is currently investigating the feasibility of regional readout and the impact on the schedule for the RD53B chip submission.

The timeline for AM08 chip submission has slipped further to October 2019. The extrapolated clock distribution power consumption was found too high and required the introduction of clock gating. As another reason for the delay, Cadence licenses became unusable, making it necessary to migrate to new software (Synopsis or Mentor).
Following the UCG recommendation to mitigate risks related to HTT, an alternative EF tracking based on commodity solutions is being investigated.

Comments

While the effort in terms of "hooks" to keep the L0/L1 evolution option feasible seemed modest at the time of the TDR, this cost is now increasing.
The estimated time scale for moving to the new AM design software seems optimistic. It is appreciated that more than a "minimal" effort seems to be devoted to the EF tracking alternative, and that the need for strong firmware management is clearly recognized.

Recommendations

- ATLAS TDAQ should converge quickly on the Cadence replacement; according to latest feedback the decision will be made by end of May (likely Synopsis).
- It is important to monitor the growth of extra costs for keeping the evolution option open, both in terms of resources and schedule.
- One should consider in advance the strategy with respect to the outcomes of the EF tracking alternative working group, in particular concerning which resources can and should be devoted in the long term, and the planning must be updated to include these resources.
- Also for the HTT, the re-baselined schedule and an update on all the main open issues should be presented at the September P2UG meeting.

Tile Project

Observations

The Phase-II project consists of the complete replacement of the on and off-detector electronics, implementing a new readout strategy, new HV and LV power systems and replacing the most degraded PMT's of the existing detector (about 1k or 10% of the total).

Since the last UCG people have been assigned to fill the remaining work-package management roles which now include a UPL Deputy, a Project Engineer and deputy leaders for all the main activities. The baseline schedule will be completed in May and now consists of 1600+ tasks in MS Project. A distilled version of around 100 of the main milestones has been compiled for the P2UG to track.

All front-end electronics PDR's have now taken place of which 3 were passed with recommendations (Active High Voltage Dividers, FE boards `FENICS' and MainBoard). The review of the Daughter board (v5) in March required a follow-up to investigate the cause of non-destructive latch-ups. These are under investigation but thought to be linked with a new FPGA version. If so, it may be required to revert back to a previous version. Irradiation tests of the FE electronics are advanced and will be completed in 2019.

Important progress is being made on LV distribution system irradiation tests and LV slow controls. LV bricks are being produced at 2 institutes where the first batch from one institute showed issues with assembly and higher temperatures than expected – this is thought to be understood and follow-up is in progress. Progress is also being made in finalizing the electrical qualification of the HV remote distribution system.

Comment:

Overall, progress towards production readiness is advancing well and the project will enter pre-production in 2019 on mechanics and some of the FE electronics components. The bigger challenge will be in integration with the DAQ, and 2019 will see important integration efforts on the full readout chain.

Follow-up

We expect to receive from ATLAS, before the summer break the final complete list of re-baselined milestones for all the projects.

Since the re-baselining process for the TDAQ (in particular the HTT) and for the ITk-Pixel projects was still ongoing at the time of this review, we asked ATLAS to include at the meeting scheduled for September 4th, specific presentations for the two projects, as mentioned in the recommendations above, in addition to the general status update report by the Upgrade Coordinator.

We agreed also with ATLAS that, in the November meeting, a preliminary schedule of the LS3 integration and commissioning activities will be presented and discussed.