WBS 6.4
LAr Calorimeter

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U.S. ATLAS HL-LHC Upgrade NSF Rebaselining and Status Director's Review
Online
Feb.28 - Mar.2, 2023

Outline

CQ-x.y

- System Overview
  - System Upgrade and U.S. Deliverables
  - WBS and Contributing Institutions
  - External Dependencies (see also risk)
- Technical Progress and Plans
  - Progress since last IPR (Aug. 2021)
  - Technical Challenges: overcome, remaining
  - Plans: review schedule, detailed goals for next year
  - Systems Engineering: interface/config management, QA/QC, ES&H
- Cost, Schedule, and Effort
  - Cost and schedule changes: rebaselining request (World Events), contingency used (Known Risks)
  - Cost and effort (costed, uncosted) profiles
  - Schedule summary: Milestones, critical path, and float
- Risk Analysis
  - Risk evolution: external dependencies, scientific effort, succession planning, supply-chain, inflation, Russia
  - Main remaining risks
  - Scope contingency and opportunity
- Responses to Previous Recommendations
  - Recommendations from previous US reviews, P2UG recommendations
- Closing Remarks

Note on vocabulary
- **World Events**: COVID, supply chain, war (included in rebaselining request)
- **Known Risks**: risks identified at FDR (normal contingency usage)

System Overview

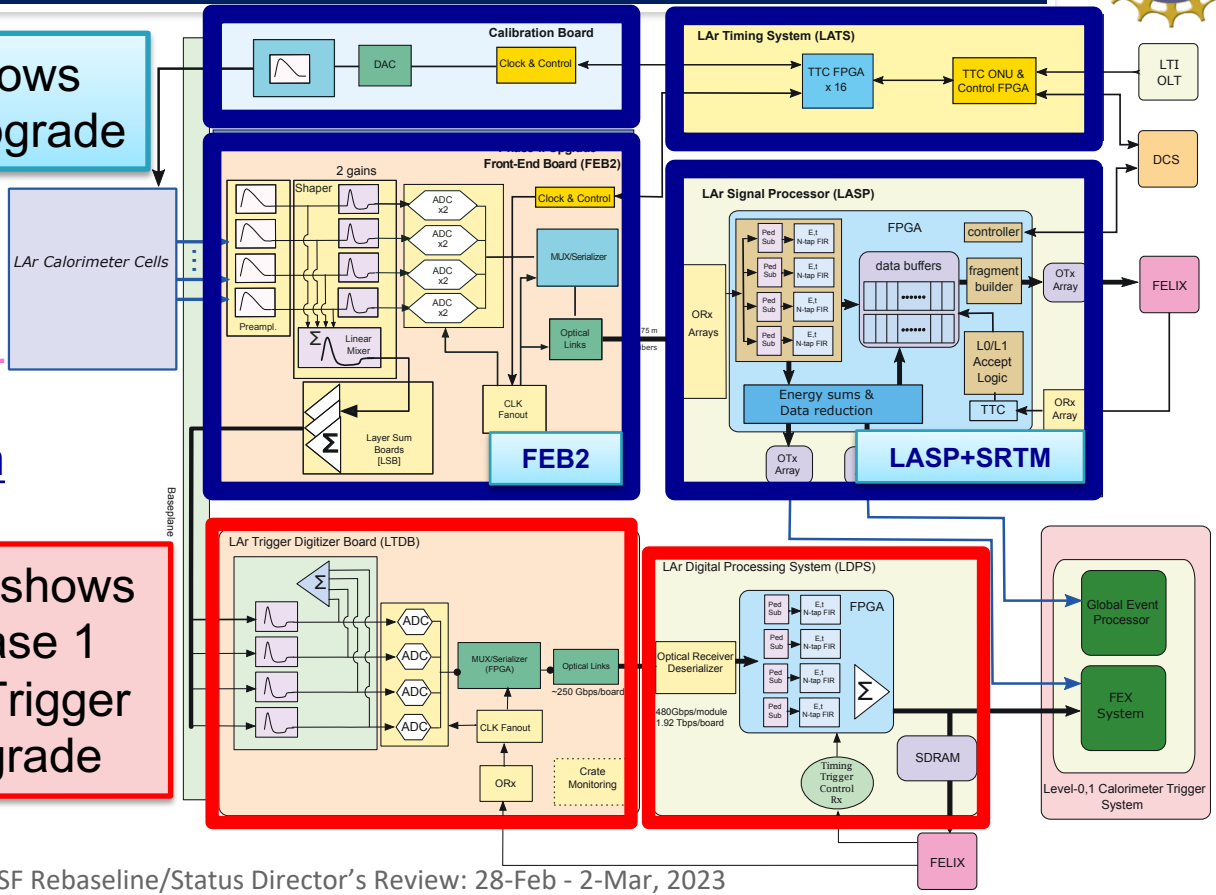
LAr HL-LHC Readout Architecture

BLUE shows HL-LHC Upgrade

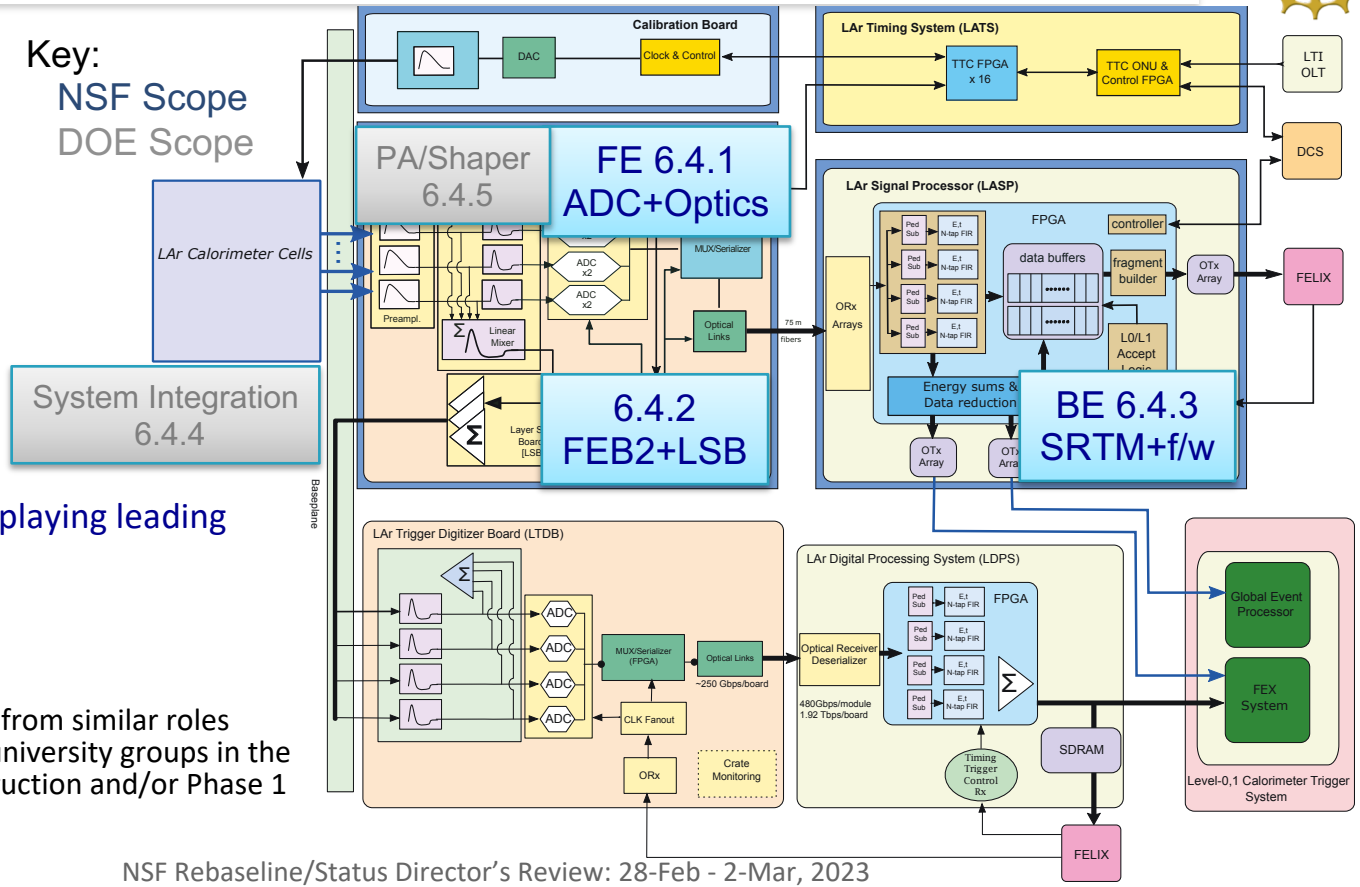
RED shows Phase 1 LAr Trigger Upgrade

Calorimeters not being changed.

LAr HL-LHC Upgrade: Full replacement of precision readout electronics



US Scope for HL-LHC LAr Upgrade



NSF Scope

- Strong university teams playing leading roles in:
  - 6.4.1 FE Electronics
  - 6.4.2 FEB2
  - 6.4.3 BE Electronics
  - Leveraging expertise from similar roles played by the same university groups in the original ATLAS construction and/or Phase 1 upgrade

NSF and DOE Scope

- LAr effort in HL-LHC upgrade project has both NSF and DOE scope
  - All LAr scope is managed together and uniformly at L2
  - Funding sources are separated at “deliverable level” (ie. WBS Level 3)
  - The NSF scope is driving the LAr HL-LHC upgrade

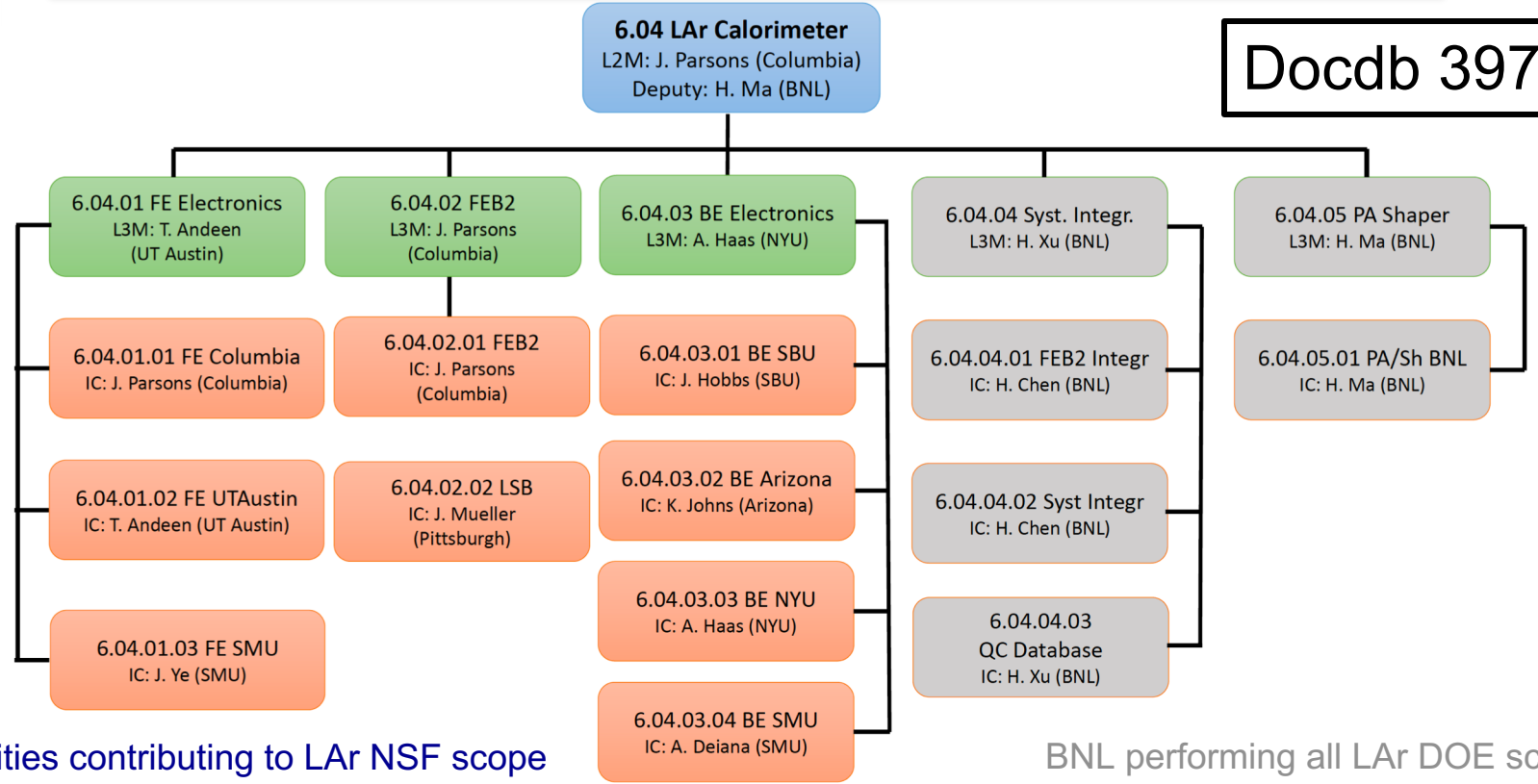
NSF Scope
  - Outlined on previous slide

DOE Scope (more details provided in Breakout Session)
  - PA/Shaper - Profiting from strength of BNL expertise (going all the way back to the invention of LAr calorimetry… up through original ATLAS construction)
  - System Integration – Profiting from BNL expertise and infrastructure, leveraging similar work done in original construction and for Phase 1 upgrade

- The boundaries between NSF and DOE scope are well-delineated and clear

WBS & Contributing Institutes

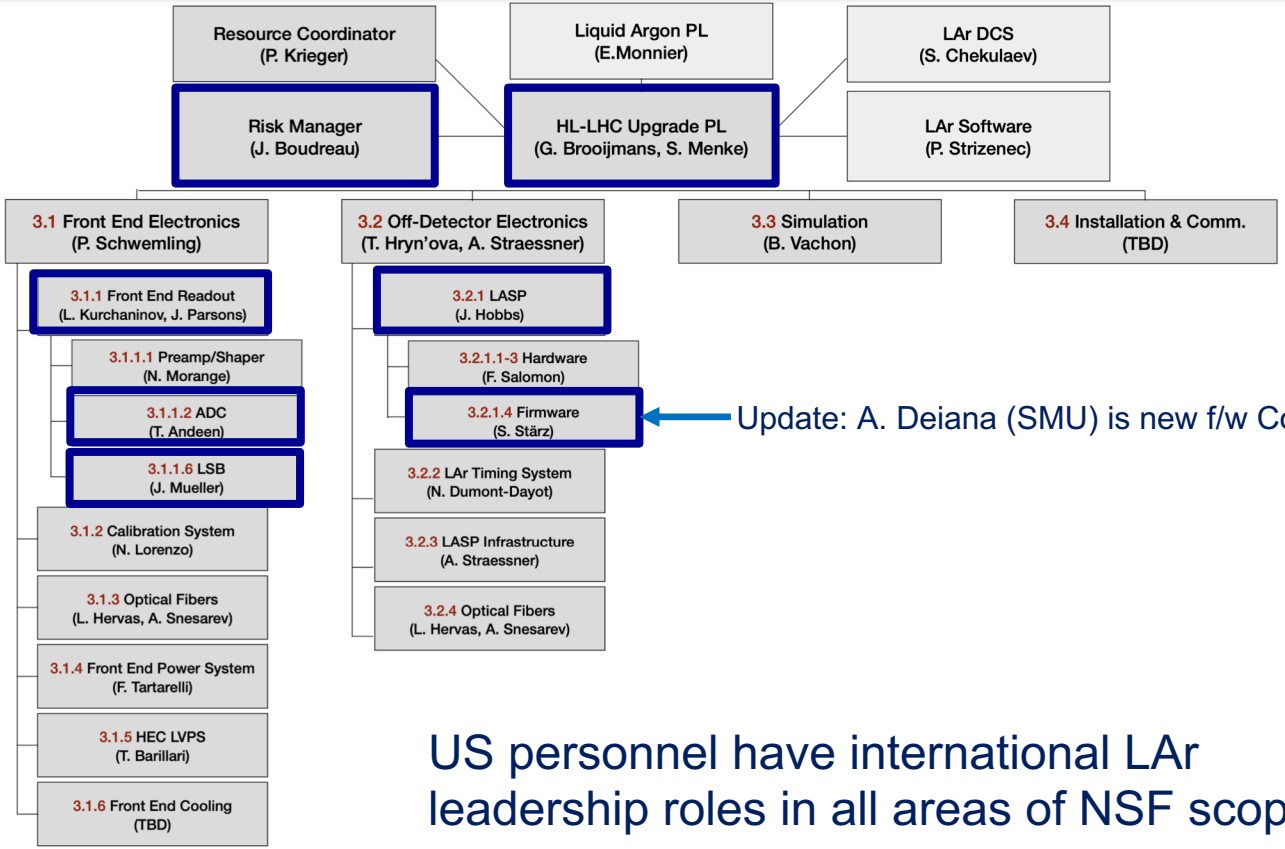
Docdb 397



7 universities contributing to LAr NSF scope
(Columbia, NYU, SBU, SMU, U Arizona, U Pittsburgh, UT Austin)

BNL performing all LAr DOE scope

International LAr HL-LHC Organization



Update: A. Deiana (SMU) is new f/w Coordinator

US personnel have international LAr leadership roles in all areas of NSF scope

External Dependencies

CQ-2.a

- 6.4.1 FE Electronics
  - Saclay to perform QC testing of 50% of production ADC ASICs (with their own robotic test system, separate from that being finalized at UT Austin)

- 6.4.2 FEB2 and LSB
  - FEB2 requires components from external partners, including custom PA/S ASICs (50:50 from BNL and IJCLab/Omega) and power devices (INFN Milano), plus ~1/3 cost sharing from collaboration
    - PA/S (like ADC) is in preproduction and well off Critical Path
    - We are working closely with INFN to finalize FEB2 powering scheme, which is on Critical Path
  - Saclay to produce and perform QC testing of 50% of production LSB mezzanines
  - As part of DOE scope, BNL to host FE Crate System Test that is key milestone before FEB2 FDR
  - BNL and Saclay to each perform analog calibration of 50% of production FEB2 boards

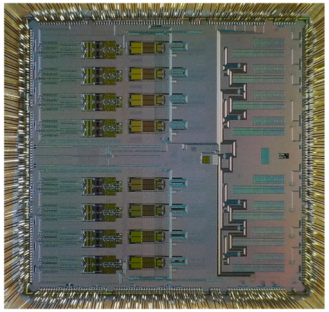
- 6.4.3 BE Electronics
  - LASP being developed by European collaborators, but SBU has produced its own SRTM Testerboard to greatly reduce external dependence
  - SRTM firmware is largely independent of LASP firmware, but of course the development must lead to a fully integrated system (A. Deiana's role as LAr HL-LHC f/w Coordinator is very useful here)

Technical Progress & Plans

6.4.1 FE Technical Progress

CQ-2.a

- Custom “COLUTA” ADC ASIC {8-chan, 40 MSPS, 15-bit, rad-tol) developed by Columbia/UT Austin in 65 nm CMOS, using 3.5-bit MDAC followed by 12-bit SAR
  - Preprototype versions v1,v2,v3 were submitted in 05/2017, 06/2018, 08/2019
  - COLUTAv4 ASIC (Final Prototype) was submitted for fabrication in September 2021
  - Original plan included 5 iterations, but COLUTAv4 already meets all specifications and is therefore the FINAL version for production (~80k chips to be produced)
  - FDR successfully held on Oct. 7/2022, after which preprod. eng. run was submitted



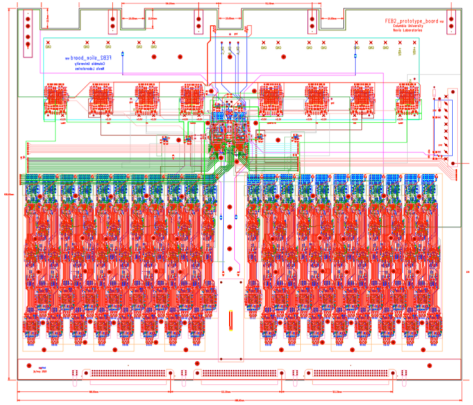
- Custom “lpGBT” 10 Gbps Serializer ASIC developed in 65 nm CMOS (including SMU contributions to chip design) for general HL-LHC use
  - QC tests underway and full production quantity should be available by mid-March
- Using lpGBT and VTRx+, SMU and Columbia developed and validated optical link design for FEB2, including redundant birectional CLK+control links and 10.24 Gbps data links
  - SMU now finalizing “splicing” of VTRx+ pigtails to improved robustness of FEB2 fiber routing

6.4.2 FEB2 Technical Progress

CQ-2.a

- With FEB2 Preprototype (“Slice Testboard”), Columbia validated FEB2 design and integrated performance of the custom components (PA/S+ADC+lpGBT+VTrx+)
  - 32-channels (of 128 for final FEB2) implemented
  - All performance requirements met
  - Redundancy of CLK/control optical links fully demonstrated
  - Boards provided to BNL, CERN, INFN Milano for further testing
  - PDR was successfully held on December 9, and greenlight given for FEB2 Prototype

- Full 128-channel FEB2 Prototype design completed and now in PCB fab
  - Uses final versions of all ASICs, in final (BGA) packages
  - Includes prototype Layer Sum Boards (LSB) from U Pittsburgh + Saclay
  - Main remaining challenge is to finalize on-board rad-tol DC-DC powering, to interface between Vin = 48V and LDOs providing final 1.2V and 2.5V
  - First version of FEB2 Prototype implements mezzanines to allow testing of multiple options, before final option is implemented on ”v2” FEB2 Prototype

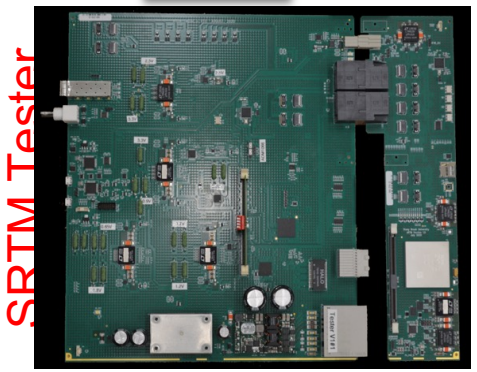


6.4.3 BE Technical Progress

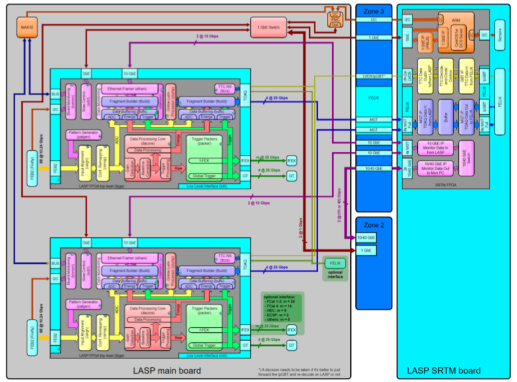
- SBU developed v1 SRTM (and SRTM Tester) and used it to validate SRTM design and integration with LASP preprototype
  - v1 SRTM required additional iteration due to change In spec of Firefly optical transceiver
  - SRTM PDR was held on January 17, 2023
  - v2 SRTM design completed and PCB fabrication is underway

View from the rear side of ATCA crate sRTM board connected to a LASP board

CQ-2.a



- Significant firmware progress has been made
  - Learning from Phase 1 experience, strengthened the f/w effort by adding manpower at NYU and SMU (in **/21 and 10/22, respectively)
  - Allison Deiana (SMU) has been appointed LAr HL-LHC f/w coordinator



Plans: ATLAS Reviews

CQ-2.a, 1.d

WBS	Deliverable	SPR	PDR	FDR	PRR
6.4.1	ADC ASIC	16-Jan-2019	08-Dec-2020	07-Oct-2022	07-Dec-2023
6.4.2	FEB2	24-Apr-2020	09-Dec-2022	22-May-2024	18-Dec-2024
6.4.3	SRTM	09-Sep-2022	17-Jan-2023	23-May-2024	20-May-2025
6.4.5	PA/S ASIC (DOE scope)	16-Jan-2019	11-Dec-2020	18-Nov-2022	26-Sep-2023

Reviews shown in green have been completed.

- Designs for both custom ASICs (65 nm ADC and 130 nm PA/S) have been successfully completed
  - Preproduction engineering runs have been submitted, with PRRs planned for this fall
- Both boards (FEB2 and SRTM) passed PDRs and are starting to fab next version
  - FDRs planned for May 2024, followed by launch of board preproduction

Plans: Next Year

CQ-2.a

- 6.4.1 FE Electronics
  - COLUTA ADC ASIC
    - Validate custom BGA package
    - Test preproduction COLUTA devices, hold PRR (12/23) and launch full production
  - Optical links
    - Purchase production lpGBT ASICs and VTRx+ modules
    - Finalize FEB2 link design, including “splicing” of multiple VTRx+ devices to MTP24 connector
- 6.4.2 FEB2 and LSB2
  - Fabricate and test v1 FEB2 Prototype board
  - Finalize design of v2 FEB2 Prototype, with final on-board powering scheme
  - Fabricate and test LSB2 Prototype (both standalone and on FEB2 Prototype)
- 6.4.3 BE Electronics
  - Fabricate and test v2 SRTM Preprototype board
  - Develop and validate firmware to integrate LASP+SRTM with FEB2 and also with TDAQ

Configuration Control

CQ-2.c

- Specifications are placed under ATLAS change control after completion of the relevant Specifications Review (SPR)
  - As shown previously, all US deliverables have successfully completed their SPR
  - Main elements for U.S. deliverables are summarized in docdb 216

- The various US LAr deliverables have not had any significant specs changes since their SPR

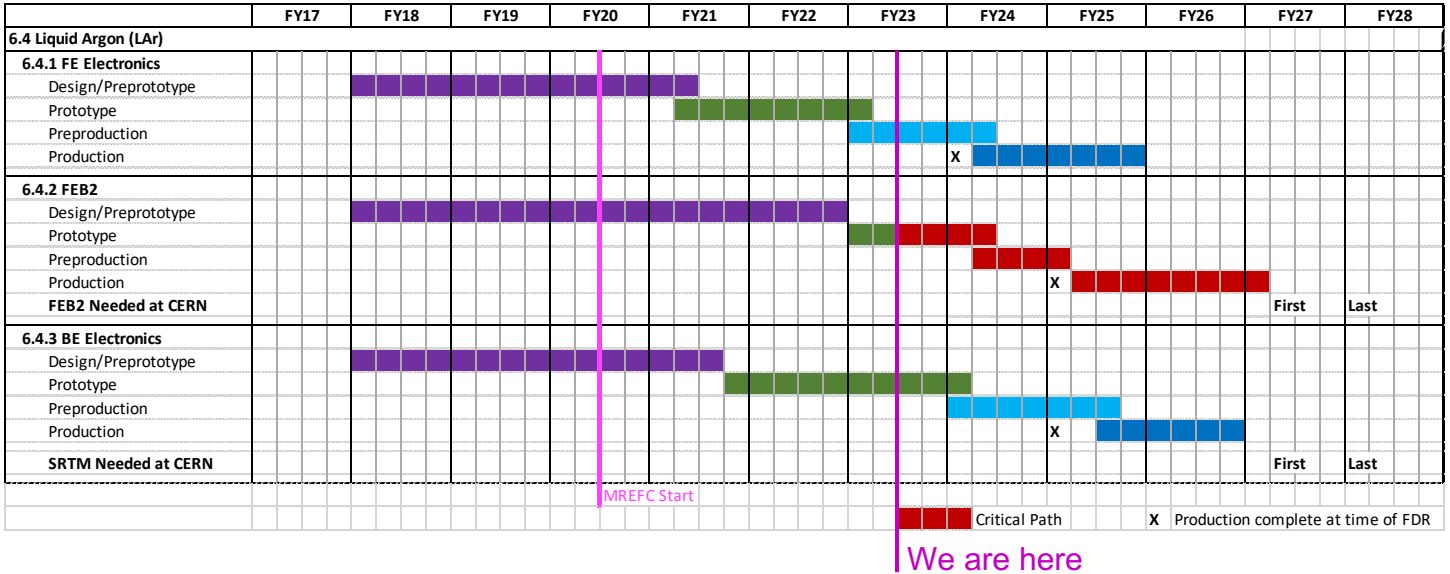
QA/QC and ES&H

CQ-2.c

- QA/QC is critical for all deliverables
  - First version of QA/QC documents have been prepared for each L3
  - QA/QC considerations are a key part of each step in the ATLAS review process:
    - Technical specifications to be achieved, including interfaces, are defined and approved in ATLAS Specifications Review, after which they go under change control
    - Demonstration of achieved QA is reviewed at ATLAS FDR before launch of preproduction
    - Demonstration of working QC process is reviewed at ATLAS PRR before launch of full production
  - QA for FE Electronics includes standalone ASIC testing and also integration testing on FEB2 boards
  - QA for FEB2 and SRTM includes standalone board testing and also integration tests in FE System Crate Test and BE System Crate Test, respectively
  - QC parameters for all deliverables will be stored and archived in "Production Electronics Database" (DOE scope is funding BNL expert to provide dB support, as done for original construction and Phase 1)
- ES&H is of critical importance
  - The BNL ES&H Liaison (Lori Stiegler) provides oversight and advice
  - Main Hazards for this L2 system
    - Electrical hazards (modest voltage but high currents) (shock, fire)
    - Material handling and rigging (eg. forklift operations)
    - Radiation: Radiation tests of electronics performed at certified facilities
      - All work done in compliance with safety policies at CERN, or at the radiation facility (eg. Massachusetts General Hospital)

Cost, Schedule, and Effort

Schedule Evolution

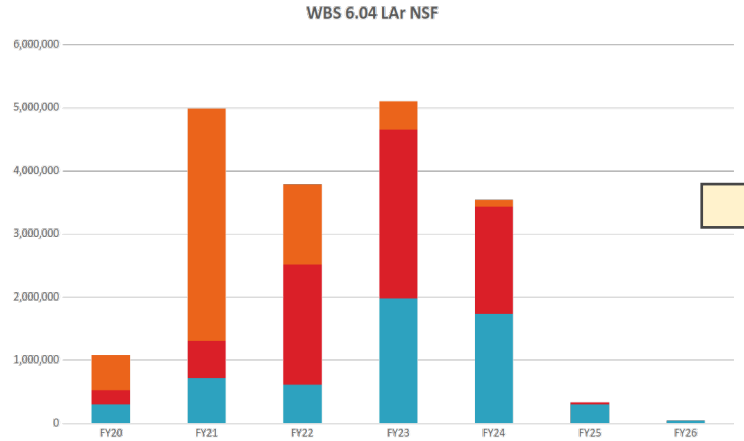


- Due mostly to "World Events", we are about 1.5-2 years behind the 2019 FDR schedule
  - Few examples: ADC FDR 4/21 → 10/22, FEB2 PDR 10/20 → 12/22, SRTM PDR 10/20 → 01/23
- During same period, LS3 has been delayed by 2 years and extended by 0.5 years
- Critical Path runs through FEB2 prototype/(pre)preproduction/testing
  - Now have 253 days of float to needed-at-CERN dates (was 220 days at FDR)
  - More detailed Critical Path schedule provided in backup

Cost Evolution

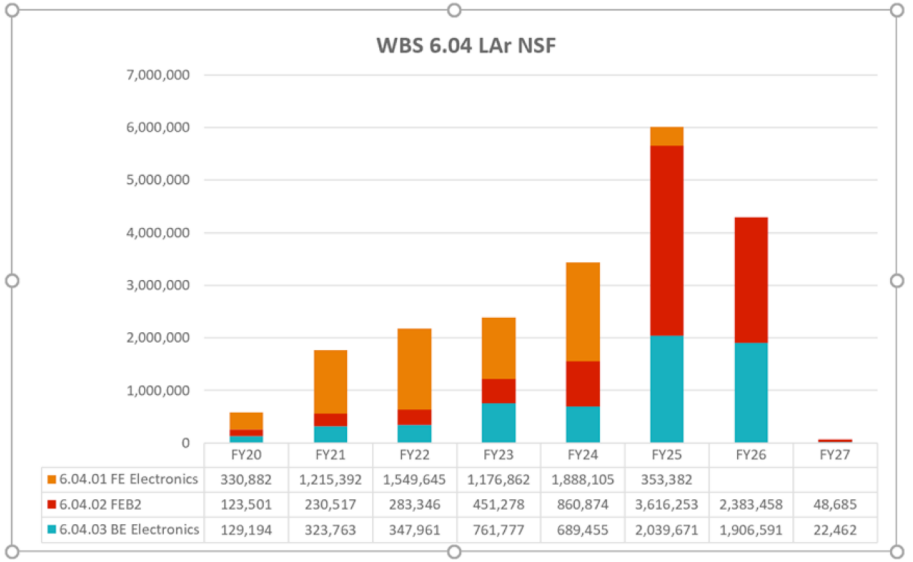
FDR (Sep-2019)

Sum of Value	FY20	FY21	FY22	FY23	FY24	FY25	FY26	Grand Total
MREFC	1,080,131	4,984,836	3,784,813	5,102,453	3,540,015	325,443	43,662	18,861,354
6.04.01 FE Electronics	553,050	3,679,117	1,270,804	441,397	105,217			6,049,584
6.04.02 FEB2	229,628	590,973	1,905,182	2,686,382	1,705,196	22,067		7,139,427
6.04.03 BE Electronics	297,454	714,747	608,827	1,974,675	1,729,602	303,376	43,662	5,672,342
Grand Total	**1,080,131**	**4,984,836**	**3,784,813**	**5,102,453**	**3,540,015**	**325,443**	**43,662**	**18,861,354**



Rebaseline (Jan-2023)

Sum of Value	FY20	FY21	FY22	FY23	FY24	FY25	FY26	FY27	Grand Total
6.04.01 FE Electronics	330,882	1,215,392	1,549,645	1,176,862	1,888,105	353,382			6,514,269
6.04.02 FEB2	123,501	230,517	283,346	451,278	860,874	3,616,253	2,383,458	48,685	7,997,911
6.04.03 BE Electronics	129,194	323,763	347,961	761,777	689,455	2,039,671	1,906,591	22,462	6,220,872
Grand Total	**583,577**	**1,769,672**	**2,180,952**	**2,389,917**	**3,438,434**	**6,009,306**	**4,290,049**	**71,146**	**20,733,052**



- Since FDR (2019), total cost has increased by from 18.86M → 20.73M (~10%)

Main Changes Since FDR

- Main drivers of Schedule changes
  - World Events
    - Had to wait 9 months for access to radn facility to radn test ADC ASIC
    - FEB2 delayed by ASICs (see above), plus about 6 months due to PCB fab/assy delays and issues
    - Had to wait 9 months to receive Zynq chips needed for SRTM preprototypes
  - Known Risks
    - Time required for development of custom BGA package for ADC
    - Increased complexity in identifying rad-tol power components for FEB2
    - Increased complexity in defining SRTM interfaces to LASP and TDAQ
- Main drivers of Cost changes
  - World Events
    - Additional manpower costs due to inefficiencies and extension of project
    - Some impact of inflation on component costs (but relatively minor)
  - Known Risks
    - Need to produce intermediate version of FEB2 Prototype, since powering not finalized yet
    - Needed additional SRTM v1.1 preprototype version due to changing spec of Firefly
    - Need more SRTM boards since baseline now 3 FEB2/LASP (instead of 4), but largely offset by cheaper FPGA prices due to CERN contracts

World Events

CQ-1.a,e

- COVID & Supply Chain impacts to NSF scope are covered in 4 BCPs
- In addition, there are 3 BCPs implementing affects of COVID changes on DOE scope
- For LAr, the total resultant cost increase is $1,069k (5.2%)

BCP #	Schedule Impact	Cost Impact (%*)	Major Changes
1033	82 – 134 days	$299k (1.4%)	COVID closures and inefficiencies, delayed ADC radn test, Zynq shortage
1038	47 – 126 days	$331k (1.6%)	Continued inefficiencies, supply chain issues
1045	40 – 143 days	$99k (0.5%)	Continued inefficiencies, supply chain issues
1057a	0 – 63 days	$403k (1.9%)	Continued inefficiencies, supply chain issues
1037, 1046,1056	0 – 60 days	$36k (0.2%)	Impact from COVID impacts on DOE scope
TOTAL	**349 - 385 days**	**$1,069k (5.2%)**	

* fraction of current L2-system base cost

Known Risks

CQ-1.a,c

- NON COVID & Supply Chain BCPs since FDR (Sep-2019)

BCP #	Schedule Impact	Cost Impact (%*)	Major Changes
1027	0 – 50 days	$389k (1.9%)	RLS adjustment before start of MREFC
1034	0	$127k (0.6%)	Add NYU firmware manpower
1041	0	-$293k (-1.4%)	Reduced cost of ADC ASIC production in 65 nm CMOS
1047	0	$332k (1.6%)	Scope opportunity: Add LSBs at U. Pittsburgh
1050	0	$188k (0.9%)	Add SMU firmware manpower
1054	0	$65k (0.3%)	Order additional die from COLUTAv4 ADC MPW for BSK pkg development
1057b	20 – 60 days	$168k (0.8%)	Non-COVID part of rebaseline BCP
TOTAL	**20 - 110 days**	**$976k (4.7%)**	

* fraction of current L2-system base cost

Large Procurements (>$100k)

Apart from PCB fab and assembly, most large procurements are placed through CERN

WBS (L3)	Item	Institution	Company	Cost (AYk$)	Obligation Date	Comments
6.4.1	ADC Production	Columbia	TSMC (via CERN)	$708k	Aug. 2022	
6.4.1	lpGBT purchase	SMU	CERN	$582k	May 2023	
6.4.1	VTRx+ purchase	SMU	CERN	$1000k	Oct. 2023	
6.4.2	FEB2 PCB fab	Columbia	TBD	$1M	Oct. 2024	Summed over full prod.
6.4.2	FEB2 PCB ass'y	Columbia	TBD	$1.8M	Oct. 2024	Summed over full prod.
6.4.3	SRTM PCB fab	SBU	TBD	$225k	Jul. 2025	Summed over full prod.
6.4.3	SRTM PCB ass'y	SBU	TBD	$110k	Aug. 2025	Summed over full prod.
6.4.3	SRTM Components	SBU	CERN + TBD	$1.9M	Aug. 2025	FPGAs via CERN

Effort Profile

CQ-2.b

- Plot and Table from PO: FDR and Rebaseline

- Scientific Effort
  - Compare FDR vs Rebaselined scientific effort
  - List reasons for any large changes
  - Discuss main use(s) of scientific effort

- Be aware of Global Risk: Loss of Scientific effort
- Be ready to discuss how your system would deal with lost scientific effort - but do not include on slides

Risks Analysis

Risk Management

CQ-1.b

- Risk and uncertainty evolution since FDR (or Aug 2021 IPR?)
  - Major realized risks
  - Main changes to risks
  - Main remaining risks
    - Explicitly mention: scientific effort, Phase-1 conflicts
  - ~~Main changes to uncertainty scores~~

- Do NOT show extracts from the RR here - but make sure the mapping from the text in this slide to RR items is clear

Responses to Previous Recommendations

Previous Recommendations

- Responses to recommendations from Aug 2021 IPR
  - Only discuss recommendations where answer is not simply “done”
- Main P2UG Recommendations affecting US scope
  - Summarize plans to address them

Closing Remarks

- NSF playing a central role in the LAr HL-LHC upgrade, with leading roles in key deliverables:
  - 6.4.1 FE Electronics – Custom ADC ASIC and optical links
  - 6.4.2 FEB2
  - 6.4.3 BE Electronics - SRTM and associated firmware
  - These deliverables were carefully chosen to leverage our expertise from very similar roles in the original ATLAS construction and the Phase 1 upgrade
- Despite the challenges of the pandemic and its aftermath, excellent progress has been made
  - Custom ADC design completed and ASIC is in preproduction, lpGBT and VTRx+ are in production
  - After successful FEB2 preprototype, entering Final Prototype phase
  - After successful first SRTM preprototype, next version being fabricated, and steady progress being made on firmware
- Since the FDR in 2019, the cost has increased 9.9% (5.2% due to World Events)
  - We currently have more float (253 d) than we did at FDR in 2019 (220 d)

BACKUP

Bio Sketch of L2 Manager

John Parsons (Professor of Physics, Columbia University)

- ATLAS roles include:
  - Since 1994, Team Leader of Columbia University ATLAS group
  - Since 12/2014, US ATLAS Level-2 Manager for LAr HL-LHC Upgrade
  - 4/2010 – 2/2017, US ATLAS Level-2 Manager for LAr Maintenance & Operations
  - Leader of Columbia Univ. group that developed and produced the Front End Board (FEB) of the current LAr calorimeter readout, as well as 5 custom ASICs
  - During original ATLAS construction, served for 5 years (‘03 – ‘08) as :
    - Member of ATLAS Executive Board and ATLAS Technical Management Board
    - LAr Electronics Coordinator
    - Member of ~10-person LAr Mgmt Group and ~20-person LAr Steering Group
  - Served for 6 yrs (‘97 – ‘03) as Co-Convenor of ATLAS Top Quark physics working group, and as member of ~20-person ATLAS Physics Coordination Board
- Previous experiments (and technical/management roles) include:
  - DZero (‘00 – ’10, LAr trigger electronics), SSC (‘91 – ’93, Leader of GEM LAr electronics), ZEUS (‘90 – ’99, Calorimeter readout electronics), ARGUS (‘85 – ’90, Microvertex detector)

Bio Sketch of L2 Deputy Manager

Hong Ma

- At Brookhaven National Lab since 1989
- Omega Group Leader, PI for BNL ATLAS research program, 2008-2016
- Physics Department Chair, 2016 - current

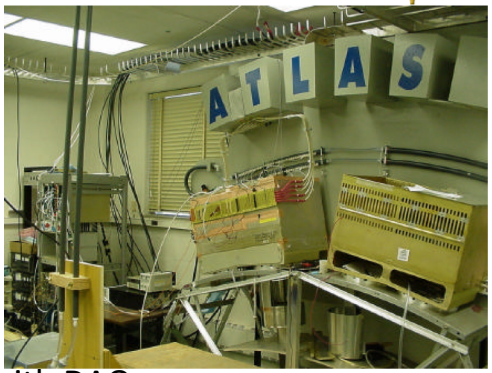
- **Experiences in ATLAS**
  - Member of ATLAS Since 1994
  - Responsible for preamp production test in ATLAS construction
  - ATLAS LAr Software and Data Preparation Co-coordinator, and member of ATLAS LAr Management Group, 2008-2016
  - US ATLAS Operations Program LAr R&D Manager 2015-2016
- **Other experiences**
  - LAr/LKr calorimeter R&D for SSC detectors, SSC Fellow early 1990's
  - AGS E865 Experiment for rare kaon decays, 1993-2000

Milestones, Critical Path, Float

- Milestone Table (L4 and above?) from PO
  - Highlight big milestones in coming ~year
- Critical Path for this system
  - Any elements close to the critical path

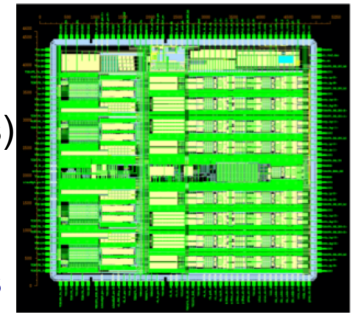
DOE Scope for LAr

WBS 6.4.4 - System Integration



- Integration tests to provide feedback to FE design and performance during FE development process
- Frontend Crate System Test, including 14 FEB2 (= 1792 chan) , LTDB, CALIB, LVPS, etc., performed to validate the FE system integration before FDRs of the various FE crate boards
- Final analog calibration and QA/QC tests of 50% of production FEB2s
- Combined system test at CERN of FE+BE electronics, plus integration tests with DAQ
- Development of QC database for US deliverables
- System Integration is critical to system development, and re-uses the BNL FE crate mockup used to perform equivalent tests during the original ATLAS construction and Phase 1 upgrade

WBS 6.4.5 – Preamplifier/Shaper ASIC



- Development, prototyping and production (in collaboration with French institutes) of custom ASIC that combines Preamp and Shaper functions
- BNL shares (50:50) responsibility with the French (IJCLab + Omega)
- PA/S is a critical component for achieving the overall analog performance specs

Timeline of COVID BCPs

CQ-1.a,e

- COVID & Supply Chain impacts to NSF scope are covered in 4 BCPs:
  - BCP 1033 – covers 03/2020 through 10/2020
  - BCP 1038 – covers 11/2020 through 04/2021
  - BCP 1045 – covers 05/2021 through 03/2022
  - BCP 1057 – covers impacts since BCP 1045, through the present time

* fraction of current L2-system base cost